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SIMULTANEOUS SWITCHING NOISE MITIGATION CAPABILITY WITH LOW PARASITIC EFFECT USING APERIODIC HIGH-IMPEDANCE SURFACE STRUCTURE

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Abstract—A novel design with low parasitic effect for eliminating the simultaneous switching noise (SSN) in high-speed circuits is proposed by using the aperiodic high-impedance surface (A-HIS) structure. The A-HIS configuration is proposed in this work, revealing suppression of the SSN from $1.1 \sim 1.85$ GHz. It is shown that the HIS structure with aperiodic design, the SSN will be effectively suppressed. The undesired resonances of the proposed A-HIS structure are less than that of the conventional structure below 1 GHz. Less undesired peaks will ensure the electromagnetic interference (EMI) and signal integrity (SI). The measured results show very well compared with the conventional periodical HIS structures. The suppression results of the proposed A-HIS structure is checked by both measurement and simulation results. By using this proposed method, the simplicity of the structure is easier to fabricate as well as to route signal lines with a perfect power/ground planes. In addition, the proposed designs provide excellent SSN suppression and good signal integrity (SI) as the conventional structure.

1. INTRODUCTION

Printed circuit boards (PCBs) for the high-speed digital circuits with fast edge rates, high clock frequencies, and low voltage levels, ground bounce noise (GBN), also known as simultaneous switching noise (SSN), on the power/ground planes has become one of major concerns. The resonance modes among the power and ground planes excited by the SSN causes serious signal integrity (SI) or power integrity (PI) problems for the high-speed circuits [1–3]. With increasing the clock frequencies, the mitigation of the SSN is becoming important.

Typical methods include the placement of the decoupling capacitors between the power and ground planes [4, 5]. These techniques centered on adding the decoupling capacitance to create a low impedance path at higher frequencies. However, this method can not provide elimination of SSN up to few hundreds MHz due to the unavoidable lead inductance. Electromagnetic band-gap (EBG) structure exhibits electromagnetic properties that have led to a wide range of applications to the filter [6, 7] and antenna [8, 9]. Recently, power plane with low period electromagnetic band gap (EBG) or photonic bandgap (PBG) structures and constant ground plane has been proposed [10, 11]. This structure exhibits wider band suppression behavior, but it could cause a SI problem and electromagnetic interference (EMI) issue. A new idea of using PBG or EBG structures embedded periodically between the parallel plates has been proposed and can provide good suppression behavior of the SSN at frequencies over few gigahertzes [12], called high impedance surface (HIS). The conventional HIS also can obtain elimination of the SSN, but this structure needed multiple cells to reach mitigation of the SSN, rendering difficulty in fabrication. The undesired resonance in low frequency also is induced by EBG and HIS structure. The EMI and SI problem will be occurred by these resonances in high-speed circuit.

In this work, an efficient method which use aperiodic concept to design the HIS structure, called A-HIS, for suppression of the PCB resonances has been proposed. To adopt the A-HIS structure instead of multiple cells of the conventional HIS structure can provide a bandgap expanding a wide range include the microwave and radio frequency. And the other hand, to compare with the conventional HIS structure, the proposed structure using aperiodic concept has a good improvement in the parasitic resonance which caused by HIS cells below 1 GHz.

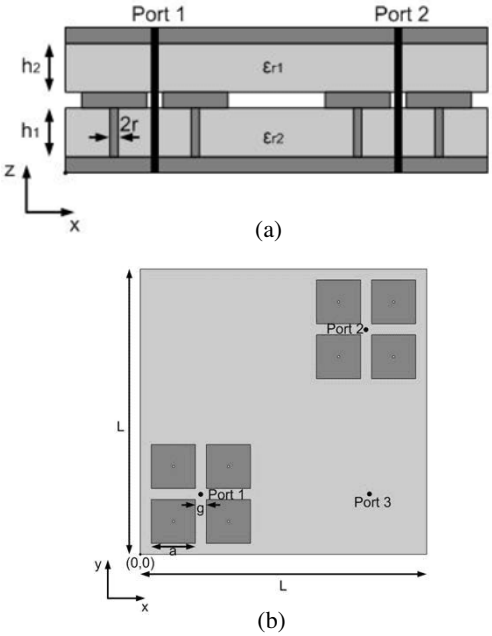

Figure 1. Schematic diagram of the proposed test boards. (a) Cross section view. (b) Top view.

2. STRUCTURE DESIGN

From SI point of view, keeping the reference planes continuous is important to obtain good signal quality. Therefore, in the proposed design as shown in Figure 1(a), the power and ground planes are kept continuous and the structures for eliminating SSN are embedded in ground plane. The dimensions of the three-layer PCB are 80 mm × 80 mm. The dielectric constant of the substrate is 4.4 with a thickness of $h_1 = h_2 = 0.8$ mm. The thickness of the metal is 0.035 mm. The top view of the HIS structure embedded in ground plane, which consists of a rectangular patch with via post positioned in its center. The corresponding parameters of unit cell are $r = 0.25$ mm, $g = 1$ mm, and $a = 15$ mm. As shown in Figure 1, three ports for the boards are located at (16.5 mm, 16.5 mm), (64.5 mm, 64.5 mm) and (64.5 mm, 16.5 mm), respectively.

3. POWER INTEGRITY AND SIGNAL INTEGRITY PERFORMANCE

3.1. Power Integrity Performance

1) *Frequency Domain*: One HIS cell around port 1 and port 2 was employed to discuss the suppression SSN behavior, as shown in Figures 2(a)–(d). The full wave simulated results are performed using Ansoft HFSS simulator. The scattering parameters of the fabricated PCB are measured with an Agilent 8364A vector network analyzer, which is connected to the SMA probes through whole structure. The reference board with power and ground planes keeping continuous is used to compared. In compared with the reference board, it is clearly seen that the one HIS cell structure behaves slight SSN suppression

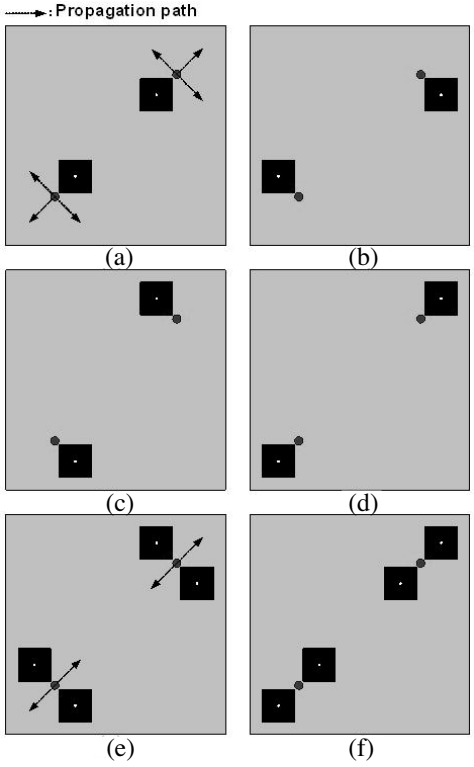

Figure 2. One and two HIS cells of the proposed structures, one cell at (a) case 1, (b) case 2, (c) case 3, (d) case 4, and two cells at (e) case 5, (f) case 6.

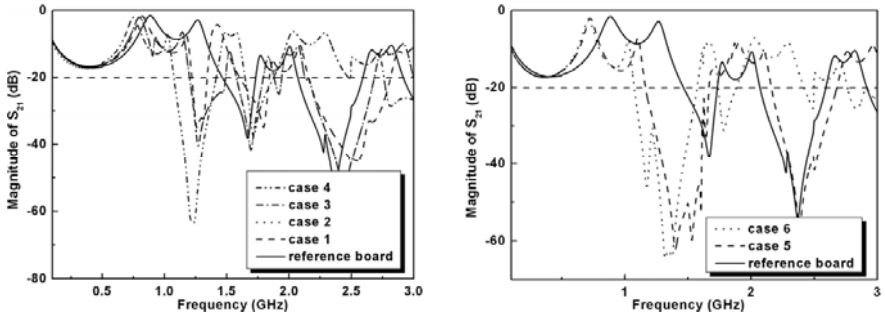

Figure 3. Comparison of the SSN suppressed by employing one and two HIS cells structure. (a) One HIS cell. (b) Two HIS cells.

with averagely 20-dB elimination in frequencies range from 1.2 to 1.5 GHz as shown in Figure 3(a). Because of three directions provided propagation path to spread SSN from port 1 to port 2, as shown in Figure 2(a). Furthermore, in the case of Figure 3(d), the elimination behavior is better than other cases due to the HIS cell was placed at the area where has larger electric filed fluctuations. And the other hand, the SSN suppression behavior employed two HIS cells around port 1 and port 2, respectively, as shown in Figure 2(e)–(f). It is observed that two HIS cells structure have wider SSN suppression than that with one HIS cell due to it isolates two directions to avoid electromagnetic waves spread, as shown in Figure 3(b). Thus foregoing cases could be seen the noise has other path to transmit signal between each port. Therefore, the efficient elimination is the HIS structure locating around the each port.

Figure 4(a) shows the SSN suppression results for the exciting port located at port 1, and the receiving port located at port 2 and port 3, respectively. It can be found that the receiving port with the A-HIS structure is efficiently suppressed the SSN than that without the proposed structure. Figure 4(b) shows measured and simulated results for the proposed A-HIS structure and the reference board, There is a little difference between measured and simulated results. That is introduced by the fabrication problems, such as the drilling via hole and the air gap between two substrates. Compared with reference board, the measured suppression results of the proposed structure are shown in Figure 5(a). The measured -20 dB stopband of the A-HIS structure is from 1.3 to 1.9 GHz, the Suppression bandwidth is 600 MHz. And the measured results of the conventional HIS structure is 1.3 to 2 GHz, the suppression bandwidth is 700 MHz. Compared

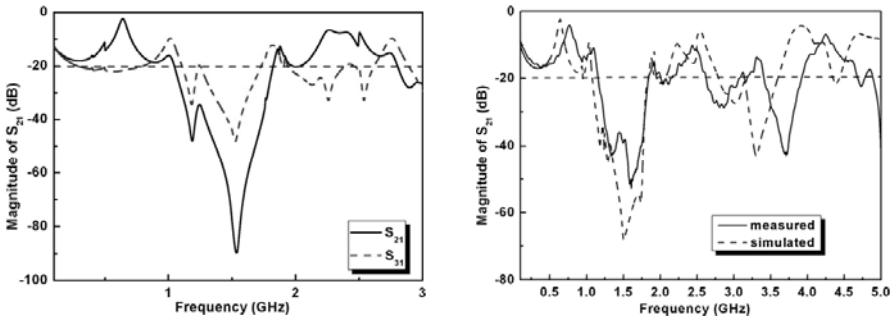

Figure 4. The SSN suppression behavior. (a) The receiving port placed at different locations. (b) Comparison between measured and simulated results.

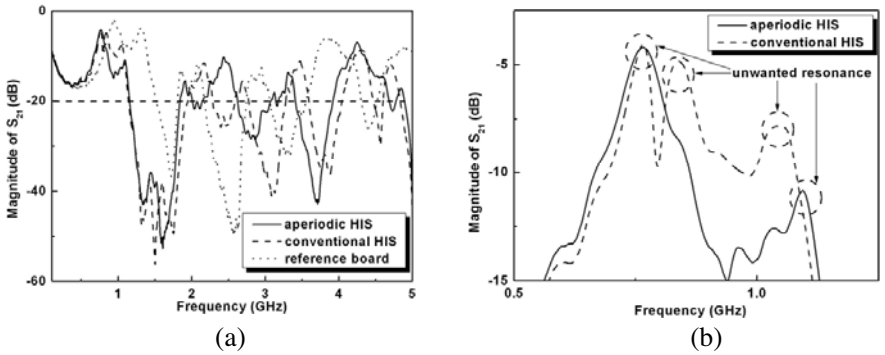

Figure 5. Comparison of S_{21} between, (a) the proposed structure, conventional HIS, and reference board by the measurement. (b) Resonances below 1 GHz.

with the reference board, it is clearly seen that the proposed structure clearly provides suppression of resonances in PCB boards. And the other hand, the EMI and SI problems induce in the proposed structure and conventional HIS structure as shown in Figure 5(b), due to the significant resonance peaks occur in low band, like as frequency below 1 GHz. The reason of these undesired peaks could be produced by the parasitic LC resonance of the HIS cell. Because of the proposed structure with the HIS cells is less than the conventional case used. Furthermore, it is clearly seen that there are three peaks with the magnitude more than -10 dB in the conventional HIS structure and only one peak in the proposed A-HIS structure. Therefore, the proposed structure is not only efficient to eliminate SSN, but also

reduces the undesired peaks to avoid the EMI and SI problems.

2) *Time Domain*: In this section, we will focus on the SSN suppression capability in the time domain for the proposed A-HIS structure. A time-domain digital current source is generated and then transformed into a frequency domain response by applying Fourier transform, as shown in Figure 6(a). The input signal is 2.5 Gbps with amplitude of 125 mV. Figure 6(b) shows the elimination behavior in time domain for the proposed structure. It is clearly found that peak coupling noise is approximately 0.022 mV, 0.02 mV and 0.12 mV for the A-HIS, conventional structure and reference board, respectively. Compared with the reference board, the SSN can be decreased approximately 83% for the A-HIS and conventional structure. It is seen that the proposed structure has good SSN suppression as the conventional structure in PI performance.

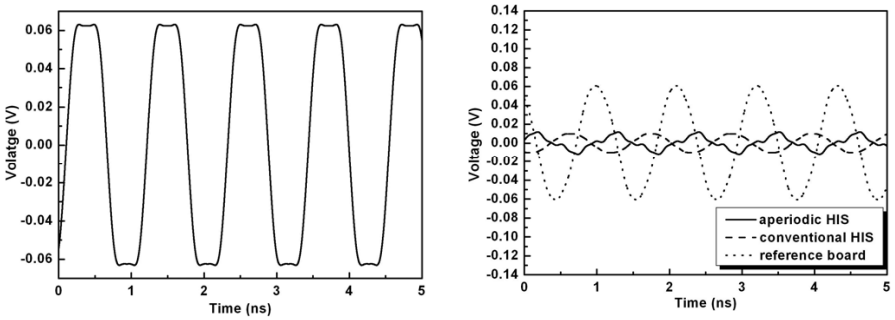

Figure 6. The SSN suppression performance in time domain. (a) Input current source. (b) Coupled noise at receiving port.

Table 1. The MEO and MEW for the reference board, conventional structure and proposed structure.

Case	MEO (mV)	MEW (ps)
Reference board	364	373
Conventional structure	359	367
Proposed structure	357	362

3.2. Signal Integrity Performance

Five layer PCB structure with signal traces through the proposed A-HIS structure is shown in Figure 7(a). The integrated power and ground plane are designed on the second and the fourth layer, respectively, and the proposed structure is designed on the third layer. The width and length of single-ended trace is 0.73 mm and 86.74 mm, respectively. The S-parameters for the proposed structure is simulated by HFSS. Afterward, the eye patterns which are used to discuss the signal quality in high-speed circuit at the output side are simulated by using pseudorandom bit sequence (PRBS) in Microwave Offices. The input signal is 2.5 Gbps with rise/fall time of 319 ps and amplitude of 500 mV. The simulated eye pattern for the A-HIS and conventional structure are shown in Figures 7(b)–(d). It is observed that for the reference board, the maximum eye open (MEO) = 364 mV and the maximum eye width (MEW) = 373 ps. Table 1 shows the compared results of three structures. Compared with the reference board, the MEO and MEW is lightly attenuated by using the A-HIS and the conventional structure. It also can be found that the SI performance

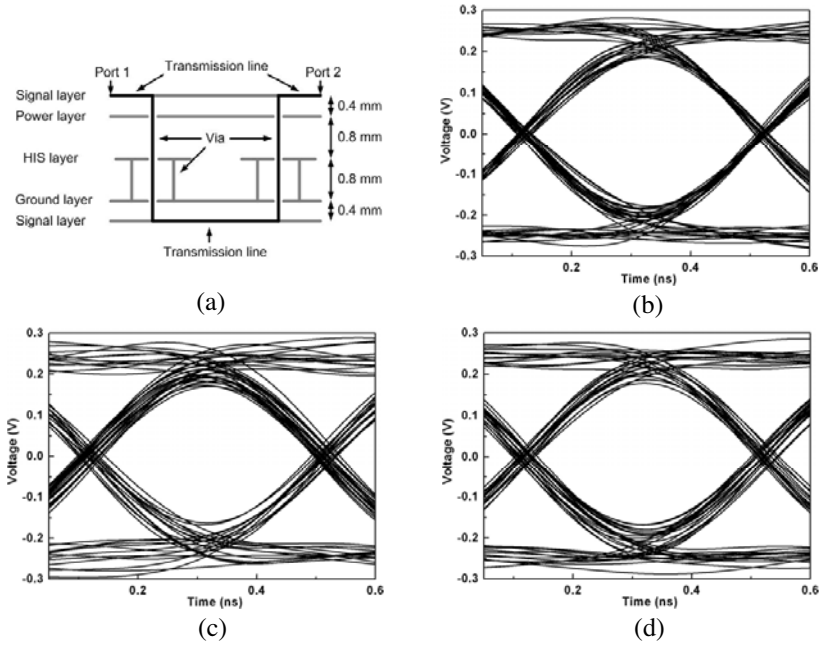

Figure 7. The results of eye pattern. (a) Five layer structure for single-ended trace. (b) The reference board. (c) The conventional HIS structure. (d) The proposed A-HIS structure.

using the proposed structure is as good as the conventional structure. It means that the proposed structure kept the good SI performance as the reference board.

4. CONCLUSION

A novel design using the aperiodic high-impedance surface structure is proposed to improve low frequency parasitic effect of the HIS structure to suppress the SSN in high-speed circuits. Compared with the conventional HIS structure, this concept just needs four HIS cells around excited and received port to obtain the SSN suppression behavior as the results of the conventional HIS. The proposed A-HIS structure also reduces the unwanted resonances in low frequency. By using this method, the simplicity of the structure is easier to fabricate as well as to route signal lines with a perfect power and ground planes. We can use the proposed structure instead of decoupling capacitance to eliminate the SSN below 1 GHz. The decoupling capacitance is not effective above a few hundred megahertz due to it will leads inductance effect. Therefore, the effectively suppressed SSN behavior below 1 GHz can be obtained by enhancement the inductance effect of the A-HIS structure. In time domain performance, the SSN can be decreased approximately 83% for the A-HIS and conventional structure. And in signal integrity analysis, the proposed structure kept a good SI performance as reference board.

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