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CHARACTERIZATION OF THE SUSCEPTIBILITY OF INTEGRATED CIRCUITS WITH INDUCTION CAUSED BY HIGH POWER MICROWAVES

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Abstract—This paper examines malfunction and destruction of semiconductors by high power microwaves. The experiments employ a waveguide and a magnetron to study the influence of high power microwaves on TTL/CMOS IC inverters. The TTL/CMOS IC inverters are composed of a LED circuit for visual discernment. A CMOS IC inverter damaged by a high power microwave is observed with power supply current and delay time. When the power supply current was increased 2.14 times for normal current at 10 kV/m, the CMOS inverter was broken by latch-up. The CMOS inverter damaged by latch-up returned its original level of functioning, because parasitic impedance inside the chip increased with the elapse of time. Three different types of damage were observed by microscopic analysis: component, onchipwire, and bondwire destruction. Based on the results, TTL/CMOS IC inverters can be applied to database to elucidate the effects of microwaves on electronic equipment.

1. INTRODUCTION

Recently, new systems that can handle large amounts of information at high speed and in remote locations are being developed. In this regard, electronic systems using digital wireless communication devices are similarly becoming more prevalent [1–6]. As the dependence on electronic systems grows, communication interference due to failure and malfunction of electronics, which are sensitive to high-power electromagnetics (HPEM) and intentional electromagnetics interference (IEMI), is becoming a serious problem [7–10]. The amount of destruction to an electronic system is determined by the amount of energy that is transferred while the electronic system is coupled by

a high power microwave. Coupling is a kind of mechanism whereby microwave energy is delivered to a equipment under test (EUT) through a circuit line. There are two modes of coupling. The first is front door coupling. Here, the microwave is directly coupled to the receiving antenna connected target. The microwave has appropriate frequency to be transmitted by a receiving channel of a system. The second is back door coupling. Here, the microwave is coupled through slits and openings into the target [11, 12].

Modern information devices can experience serious failures and malfunction because of thermal secondary breakdown caused by high power microwaves, as devices are mostly comprised of integrated circuits and microelectronics, which are sensitive to microwaves. This is caused by over current when the reverse voltage is biased to the PN junction region [13]. Consequently, study of the effects of microwaves on information instruments is needed. This research examines the destruction and malfunction of semiconductor devices caused by high power microwaves.

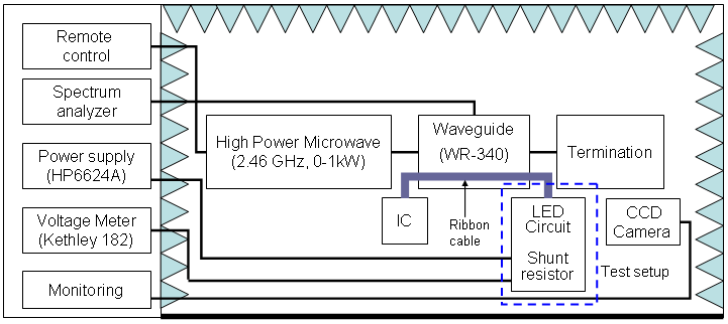


Figure 1. Schematic of experimental setup to produce high power microwaves.

2. EXPERIMENTAL

A magnetron was used to generate HPM in the experiment. Figure 1 shows the experimental equipment set up to gather and analyze data on destruction and malfunction of TTL/CMOS IC inverters by the impact of a high power microwave. The high power microwave generated from the magnetron is connected to a launcher, which transports it through a waveguide (WR-340) [14]. The high power microwave is transmitted through the waveguide and a ribbon cable linked to the CMOS inverter. To eliminate the heat caused by the high power microwave, a cooler is used in termination to cool.

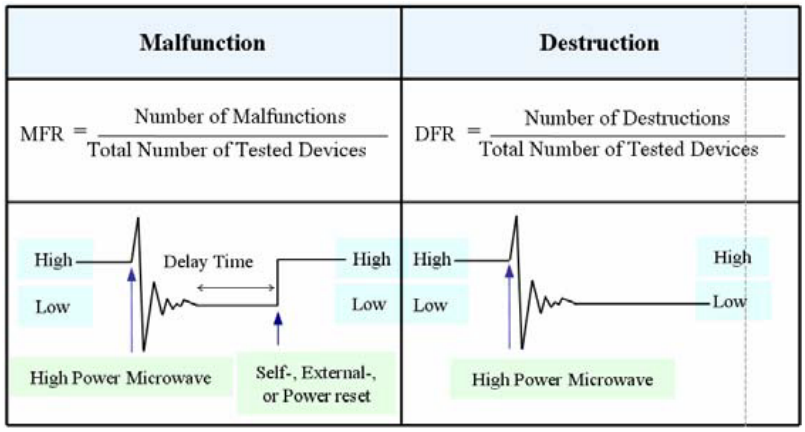


Figure 2. Definition of malfunction and destruction.

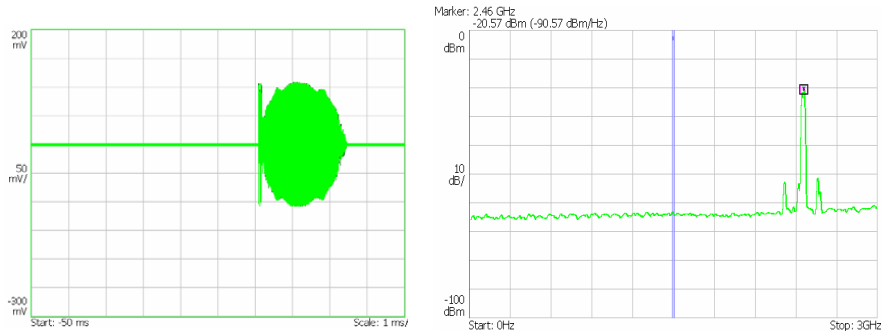
Figure 2 defines the potential malfunction and destruction to TTL/CMOS IC inverters by high power microwaves [15]. In this case, malfunction does not mean physical damage. After resetting (self-, external- or power reset), the original functions of the system can be recovered. The Malfunction Failure Rate (MFR) is defined as the number of malfunctions of the system divided by the total number of tested devices to the system. Destruction refers to physical damage of the system. Here, the system can not be restored to function again. The Destruction Failure Rate (DFR) is defined as the number of destructions divided by the total number of tested devices. Four quantities (MT; Malfunction Threshold, MR; Malfunction Range, DT; Destruction Threshold, DR; Destruction Range) were defined parameters for the description of the susceptibility of a system [15].

Four different semiconductors (two TTL-, two CMOS-families) have been tested in terms of their susceptibility to high power microwaves. Inverter logic devices were chosen to observe the influence of the manufacturing technology on the malfunction and destruction effects.

Two methods were used to confirm the phenomena of malfunction and destruction when high power microwaves were transmitted via a ribbon cable linked to an IC inverter. The ribbon cable is connected IC inverter and LED circuit via a waveguide, and the test setup has formed a LED circuit. Malfunction in the IC inverter can be measured by abnormal LED circuit behavior. Another method of surveying the characteristics is to measure the power supply current, because its malfunction was caused by an increase of the power supply current [16].

Also, delay time was examined for the IC inverter recovery from the malfunction. The condition of the internal chip of the semiconductor after exposure to a high power microwave was studied using an optical microscope.

Classical HPM generators such as magnetrons, BWO, and Klystron produce output signals at fixed frequencies in a rise time range of 10–100 ns. Figure 3 shows the time domain and the frequency domain of a HPM of a magnetron with a frequency of 2.46 GHz.



(a) Time domain (b) Frequency domain

Figure 3. The time domain and frequency domain of the HPM signal.

3. RESULTS AND DISCUSSION

Figure 4 shows the DFR of IC inverters made via two different TTL technologies. The DT (Destruction Threshold) of the TTL inverters is about 8 kV/m and 12.2 kV/m, respectively, and the DR (Destruction Range) of the TTL inverters is in a range of 8 kV/m to 8.6 kV/m and 12.2 kV/m to 12.5 kV/m, respectively. Figure 5 shows the DFR and BFR for IC inverters built in two different CMOS technologies are affected by high power microwave. The DT of the CMOS IC inverters is 9.2 kV/m and 11.9 kV/m, respectively, and the DR of CMOS inverters is in a range of 9.2 kV/m to 9.5 kV/m and 11.9 kV/m to 12.5 kV/m, respectively. Also, the MT (Malfunction Threshold) of the CMOS IC inverters is about 6.4 kV/m and 9.3 kV/m, and the MR (Malfunction Range) of the CMOS IC inverters is in a range of 6.4 kV/m to 7.2 kV/m and 9.3 kV/m to 10.3 kV/m.

Thus, the TTL IC inverters experienced non-reversible destruction, and malfunction did not occur, in contrast with the CMOS IC inverter. However, the CMOS IC inverters were recovered by switching

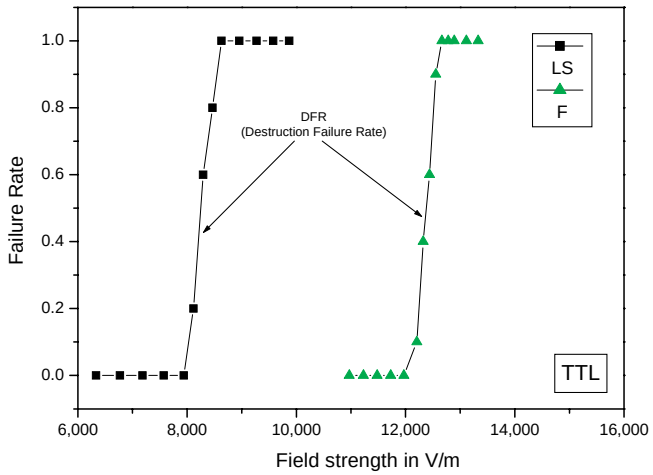


Figure 4. DFR (Destruction failure rate) of TTL IC inverters by impact of high power microwave.

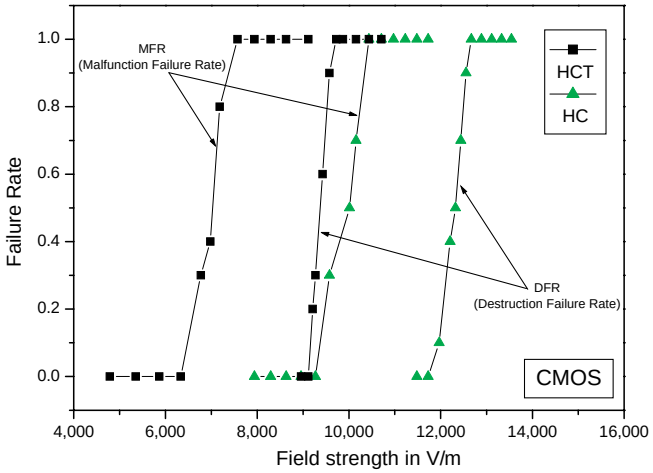


Figure 5. MFR (Malfunction failure rate) and the DFR (Destruction failure rate) of CMOS IC inverters by impact of high power microwave.

the power off/on again. This effect can be explained by the parasitic thyrister near the N and P type channel transistors inside the CMOS IC inverter. Such damage to TTL/CMOS IC inverters corresponds with previous experiment results [15]. Also, based on results of the experiment, malfunction of CMOS IC inverters occurred as follows. If

the MFR is smaller than 1, it is impossible to predict whether malfunction will be produced by high power microwave. In this case, malfunction affecting the CMOS IC inverters is irregular. Malfunction of the CMOS IC inverter occurs when a certain critical field strength is exceeded. The critical value of the field strength is dependent on many factors. First, there are constant influencing factors such as chip fabrication technology and chip layout of the CMOS IC. Also, there are variable factors such as switching states of the transistor. Because of these uncertain outcomes, the critical value of field strength varies randomly [17]. Therefore, the effects on semiconductors in terms of malfunction and destruction could be more concretely identified by defining the failure rate in accordance with the field strength. Figure 6 shows the malfunction and destruction failure range of inverter devices built with four different technologies.

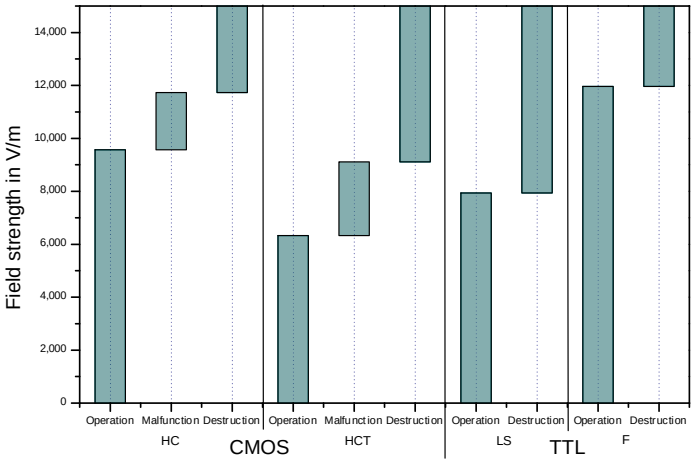


Figure 6. Malfunction and destruction failure range of CMOS/TTL inverters by impact of high power microwave.

Figure 7 shows the change in power supply current of the CMOS IC inverter upon malfunction of the inverter as a result of a high power microwave. As shown in the figure, the power supply current rapidly increases from 28 mA to 75 mA when the field strength reaches approximately 6.8 kV/m. The power supply current increases about 2.6 times in the case of the HCT-CMOS inverter relative to a normal current. Also, at the point where malfunction first occurs, the power supply current rapidly increased for 1 sec and recovered to the original condition. However, at the point where malfunction took place for the second time, the power supply current maintains increased state until

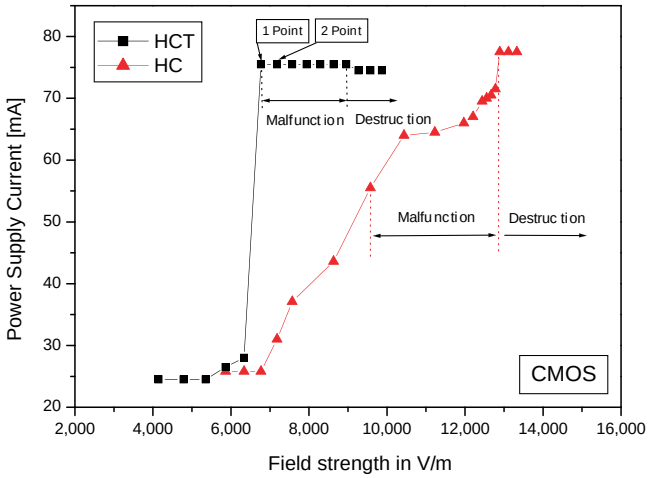


Figure 7. Power supply current of CMOS inverter by impact of high power microwave with field strength.

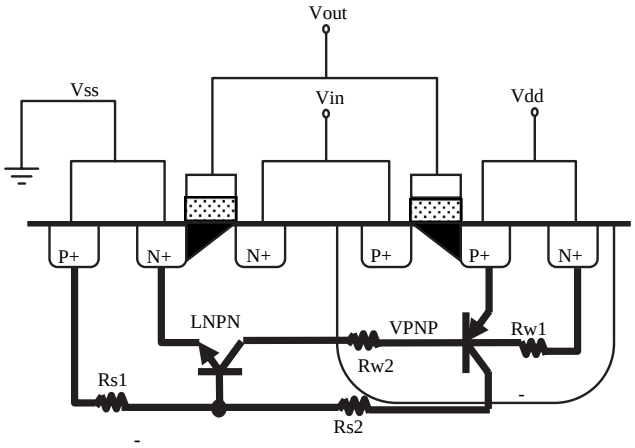


Figure 8. Parasitic bipolar components of PNPN structure.

the power supply was shut off. The result was considered to be caused by a latch-up phenomenon due to parasitic bipolar components near the N and P type channel transistors in the CMOS device. Latch-up is a phenomena where impedance between the power supply and ground becomes low, and when a vertical PNP (or NPN) transistor and lateral NPN (or PNP) transistor, which create a parasitic PNPN bipolar structure, simultaneously operate. When latch-up occurs, a

large amount of current suddenly flows between the Vdd and Vss. The current causes malfunction or destruction of the CMOS device. To examine the latch-up of the CMOS, the 4-terminal structure schematically illustrated in figure 8 was used. Here, R_{w1} is the parasitic resistance between the emitter base of the PNP and R_{s1} is the parasitic resistance between the emitter base of the NPN. VPNP denotes the vertical PNP transistor and LNPN denotes the lateral NPN transistor. The latch-up phenomena did not occur in the HC-CMOS, because HC-CMOS device had improved defect by which latch-up well arise.

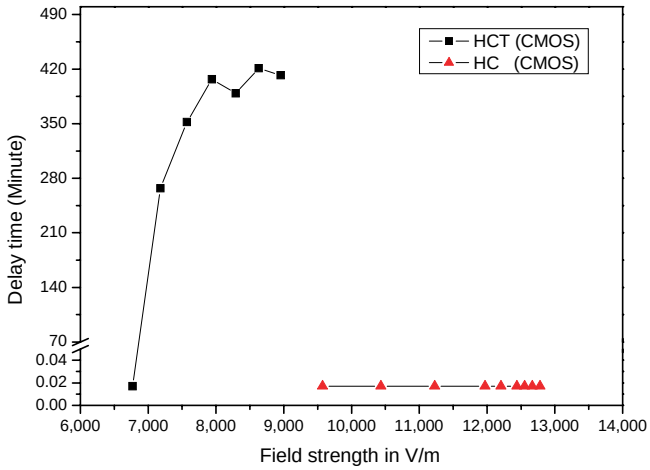


Figure 9. Delay time of the CMOS inverter from malfunction.

Figure 9 shows the delay time of CMOS inverters with the field strength within the malfunction range. The delay time of the HCT-CMOS inverter with increased field strength was extended greatly, from 1 second to 407 minutes, and then levelled off. However, the delay time of the HC-MOS inverter is very short.

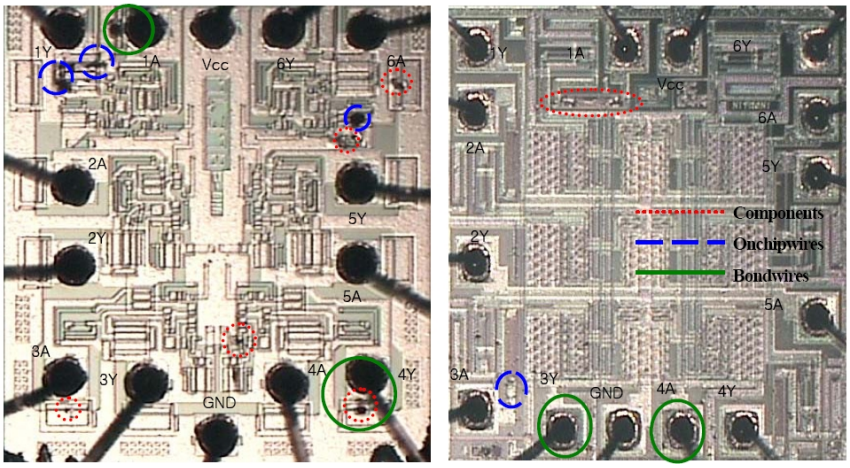
As a result of the high power microwave, inductive current caused latch-up given to substrate or well. To maintain the latch-up condition of the circuit, more current than the holding current must be supplied. Since both bipolar transistors in the latch-up condition have to operate in the saturation region, the holding current can be explained by the following equation [18].

$$I_h = \frac{\beta_p(\beta_n + 1)I_{rw} + \beta_n(\beta_p + 1)I_{rs}}{\beta_p\beta_n - 1}$$

Here, I_{rw} and I_{rs} are the current flowing to R_{w1} and R_{s1} in the emitter base of the transistor, and the holding current is inversely proportional

to R_{w1} and R_{s1}. If the holding current is increased because of the high power microwave, latch-up occurs as both R_{w1} and R_{s1} inside the semiconductor decrease. Also, operation of the semiconductor is restored to the original level, because both R_{w1} and R_{s1} inside the semiconductor increase with time.

An internal chip analysis of destructed semiconductor was carried out using an optical microscope. Figure 10 shows the TTL/CMOS inverters after exposure to a high power microwave with a maximum field strength of about 13.5 kV/m. The inverter device is separated into six single inverter gates each with an input (A) and an output (Y). Additionally, there are two connectors for the supply voltage (Vcc) and the ground (GND). The distribution of the destruction on the chip indicated that the primary destruction was to the inverter gates in the Vcc and GND sides.



(a) F-TTL inverter (b) HC-CMOS inverter

Figure 10. Damage to inverter devices by high power microwaves.

A microscopic analysis of the inverter devices statistically shows three different levels of damage, as indicated in Figure 11. The damage became more severe with increasing field strength. The effect on the TTL/CMOS inverter was similar to other experiment results [19]. At a field strength of level 1, more than 11.9 kV/m component destruction on the chip occurred, mainly as a result of flashover effect. When field strength of level 2 was increased beyond 12.6 kV/m, melting processes mainly damaged the IC-lines. A field strength of level 3 exceeding 13.1 kV/m led mostly to bondwire destruction.

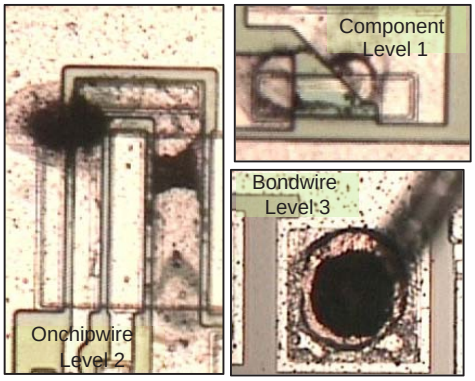


Figure 11. Damage at the field strength level.

Table 1. Tested TTL/CMOS gate families.

TTL(Transistor Transistor Logic)
• Low Power Schottky(LS)
• Fast (F)
CMOS(Complementary Metal Oxide Semiconductor)
• High Speed (HC)
• High Speed-TTL Inputs (HCT)

4. CONCLUSION

The susceptibility of different types of inverter devices and the delay time of the CMOS devices that experience malfunction varied according to different breakdown effects. The CMOS inverter devices underwent reversible malfunction, which could be reversed by resetting. However, the TTL inverter devices showed only irreversible physical destruction. These malfunction effects occurred due to the parasitic thyrister near the N and P type channel transistors. Also, by defining the malfunction and destruction according to the field strength of the semiconductor device, the field strength at which malfunction and destruction occur can be identified. At the point where the field strength was about 6.8 kV/m, the supply current rapidly increased from 28 mA to 75 mA. The power supply current increases about 2.6 times relative to the normal current. The cause of failure is attributed to a latch-up phenomenon due to parasite bipolar component near

the N and P type channel transistors in CMOS device. The latch-up phenomena did not occur in the HC-CMOS inverter. The increase of the field strength extended the delay time significantly, from 1 second to 407 minutes, and then levelled off. The semiconductor recovered its original operation level, because the impedance inside the semiconductor increases with time. The destruction effects can be classified as component, onchipwire, and bondwire destruction. This investigation can be applied to database to elucidate microwave effects of electronic equipment.

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