Progress In Electromagnetics Research Letters, Vol. 1, 189–196, 2008

ANALYSIS OF CAPACITANCE ACROSS INTERCONNECTS OF LOW-K DIELECTRIC USED IN A DEEP SUB-MICRON CMOS TECHNOLOGY

A. Sonanvane, B. N. Joshi, and A. M. Mahajan

Department of Electronics
North Maharashtra University
Jalgaon-425001, India

Abstract—The paper presents the detailed analysis of the interconnect capacitance, crosstalk time and peak crosstalk voltage. The dependency of the couple capacitance and fringe capacitance on the interconnect layer dimensions affects significantly to the interconnect capacitance. The peak crosstalk time obtained to be 13 femtoseconds for 9.6 femtoseconds of propagation delay, while the maximum crosstalk voltage obtained to be 178 mV.

1. INTRODUCTION

The integrated circuits (IC) chip size, complexity, and device packing density continuously increases with the advances in technology [1, 2]. New techniques have resulted in reduction in the minimum feature size used in the IC'S. At the same time, improvements in materials technology have allowed integration of more and more devices on the same chip, resulting in increased area. According to theory of scaling [3–6], the smaller dimensions of an MOS transistor should enhance its speed. The cause of gate delay increase is that drain current decreases at low supply voltages. Furthermore, gate delay is increased by the higher junction capacitance at low supply voltage, because the depletion layer width becomes thin. In order to reduce the gate delay, high current drivability and low source/drain junction capacitance are indispensable. The physics governing the transistor favors this size reduction, the performance of the wires used for electrical interconnects does not significantly improve using this type of scaling. Thus, a new approach to signaling and clock distribution will be needed to take CMOS [7, 8] circuit performance beyond the limits imposed by electrical interconnects [9–13]. The low-k dielectric [14] interconnects

have the potential to circumvent these limitations, provided a number of technological issues can be addressed.

As we continue to exploit deep submicron (DSM) technologies to design faster and smaller circuits, we must revisit the problem of calculating the gate propagation delay. With shrinking in device size the complexity of interconnect structure increases requiring multilevel interconnections to realize high performance and high functionality integrated circuits. However, the use of multilevel interconnections increases signal propagation delay and cross-talk in devices using conventional metal (Al) interconnects and silicon dioxide (SiO2) as the Interlayer Dielectrics (ILD) [15, 16]. The parasitic resistances and capacitances associated with such a contact technology severely degrade the device performance. Methods of reducing the source/drain area and hence the parasitic elements have been studied extensively. An increasingly method is to extend a low-resistivity and low-k dielectric materials allowing the contact to overlap onto, or be completely on the field oxide as shown in the following Figure 1. Hence, we had carried out the analysis of various structural and electrical parameters such as the parasitic capacitance, crosstalk, and line signal [17, 18]. The paper has four sections; the following section two describes the brief experimental process, while section three has been dedicated for the results and discussion finally in section four we presented the concluding remarks.

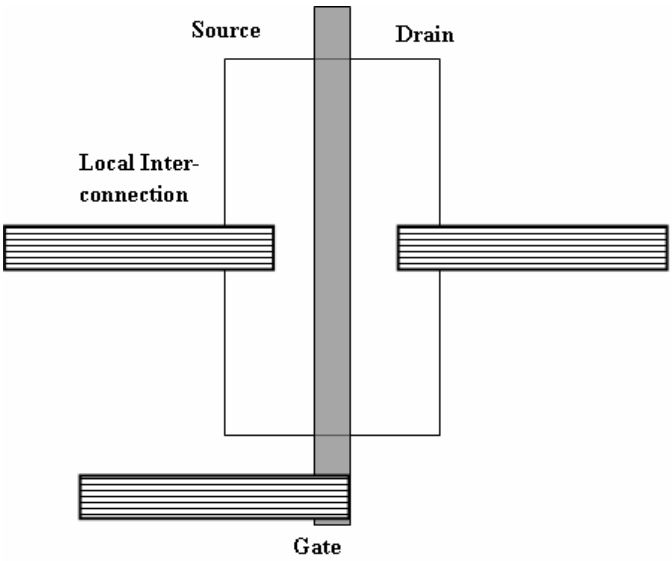

Figure 1. Schematic diagram of transistor with local interconnection.

2. THEORETICAL MODEL

The low dielectric constant (k) materials are in the great demand as they are being used as ILD [18–20] for reducing parasitic capacitance and power dissipation in ULSI devices. The miniaturization of active passive devices in a modern microelectronics has led us to investigate for the new low-k dielectric materials which plays a vital role to reduce the capacitive delay, crosstalk noise, and therefore, improves the performance of the devices drastically.

It has been observed that the efficient performance of the VLSI can be achieved by reducing RC delay. Hence, we had focused on the dependence of capacitance of various structural and material parameters. The total capacitance is the summation of the coupled capacitance and area fringe capacitance i.e.,

$$C_{Total} = C_{cou} + C_{af} \tag{1}$$

where the suffix 'cou' is for couple, while the suffix 'af' denotes area fringe. The coupled capacitance is the function of the structural parameters of the interconnect layers which is given by the following expression.

$$\begin{aligned} C_{cou} \;=\; & E_{ox} * (1.144 * t/s) * \left(A_1^{0.0944}\right) \\ & +0.7428 * \left(B_1^{1.144}\right) + 1.158 * \left(C_1^{0.1612}\right) * \left(D_1^{1.179}\right) \end{aligned} \tag{2}$$

Here, 't' is the thickness of the interconnect wire, A_1, B_1, C_1 and D_1 are structural parameters based variables. Similarly the area fringe capacitance is given by the following relation.

$$C_{af} = E_{ox} * (w/h + (2.217 * A) + (1.171 * B) * C) \tag{3}$$

Again here A, B, C and D are the structural parameters dependent variables; E_{ox} is the permittivity of low-k dielectric material SiCOH. 's' is the interwire spacing, w is the width of interconnect and h is the height of interconnect. A detailed analysis of the capacitance which shows great dependence on interconnect dimensions has been analyzed in the following section.

3. RESULTS AND DISCUSSIONS

It is important to observe from Figure 2 that interwire spacing is a very crucial structural parameter which drastically increases the total capacitance when the interlayers are closely packed. Hence, we are forced to increase the interwire spacing which reduces the

packing density of VLSI, greater area of the wafer is required, length of interconnects are increased which results in the enhancement of the resistance and certainly the power consumption suddenly rises. Interconnect total capacitance at any node contains three components: overlap capacitance, lateral capacitance and fringe capacitance. The fringe capacitance arises from the coupling of two conductors through the interconnect layers.

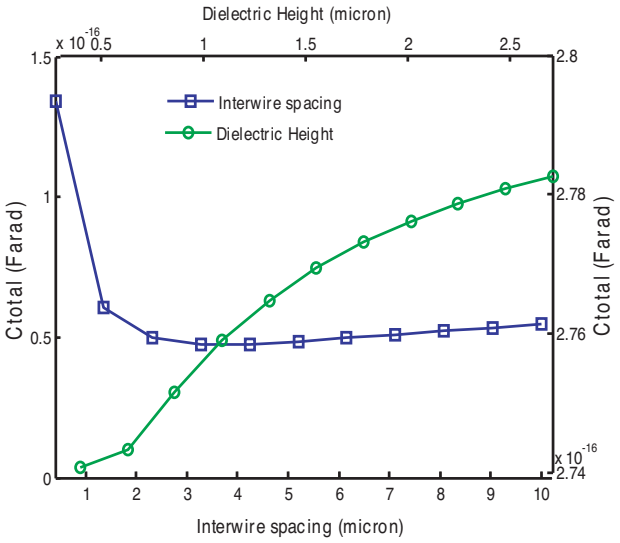

Figure 2. Total capacitance variation across interconnect layers of SiCOH.

Apart from the other capacitance contributions the interconnect capacitance depends on the interwire spacing and dielectric height. In Figure 2 a nonlinear variation of interconnect capacitance has been observed for the varying interwire spacing and dielectric height. The interspacing of 3 micron and dielectric height of 1.25 micron provides a proper compensate value of the interconnect capacitance. Since the parasitic capacitance is directly proportional to the area of fringe and couple capacitance, the total capacitance increases with the increase in dimensions of interconnect.

The Figure 3 shows the linear variation of the total capacitance for the varying wire thickness and wire width. The wire thickness has been increased up to 1.2 micron while the wire width is varied up to 2 micron, the peak capacitance has been observed for these two maximum values of the thickness and width of the wire. The increase in the total capacitance is attributed by the increase of a

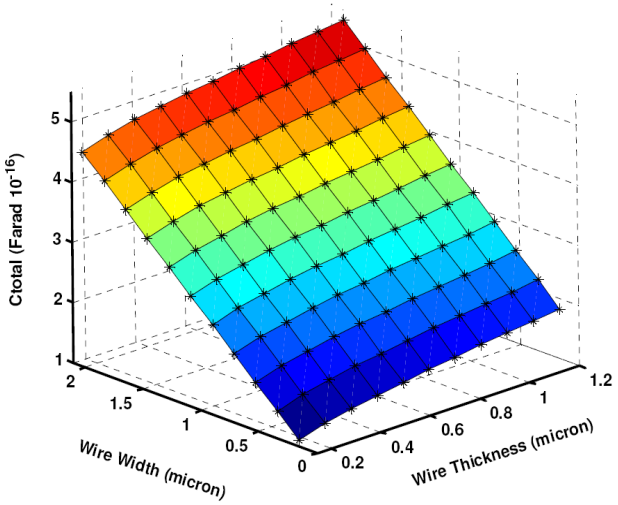

Figure 3. Simultaneous variations of wire width and thickness to study interconnect capacitance.

coupling capacitance and area fringe capacitance with the increase of the wire width and wire thickness. The area fringe is found to be smaller as compared to the coupling capacitance appears to the parasitic capacitance. Therefore, to improve the performance of the VLSI chip the dimensions of interconnects also plays a vital role.

The propagation delay is the function of the input transit time and output load. Hence, for reducing the transit time and output load the optimization of interconnect dimensions are required. Thus, the importance of the propagation delay due to internal resistance and the various parasitic capacitances has force us to realize the peak crosstalk time with respect to propagation delay. In Figure 4, the linear increase in peak crosstalk time as a function of delay time has been depicted. The increase in the RC delay time enhances the parasitic capacitance and resistivity which introduces the crosstalk and noise in the integrated circuits. It has been revealed in the following figure that the peak crosstalk time increases from 6 femtoseconds to 13 femtoseconds for the corresponding values of delay time from 4.8 femtoseconds to 9.6 femtoseconds.

The concern about delay times on the chip and crosstalk between the components and signal traces has forced the researchers to investigate about the crosstalk time and the voltage occurs due to crosstalk time. The better designing of the VLSI deals with number of parameters amongst which interconnect and crosstalk time has been

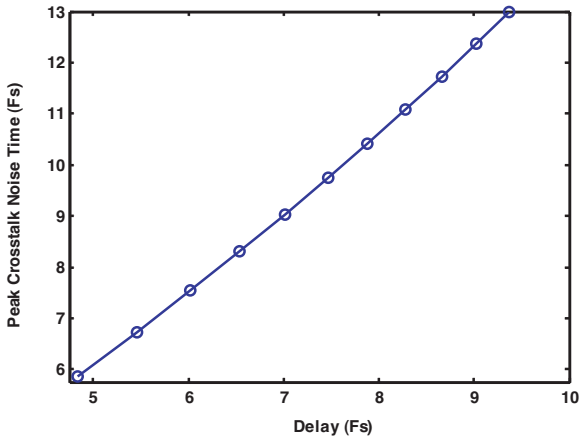

Figure 4. Peak crosstalk time variation with propagation delay.

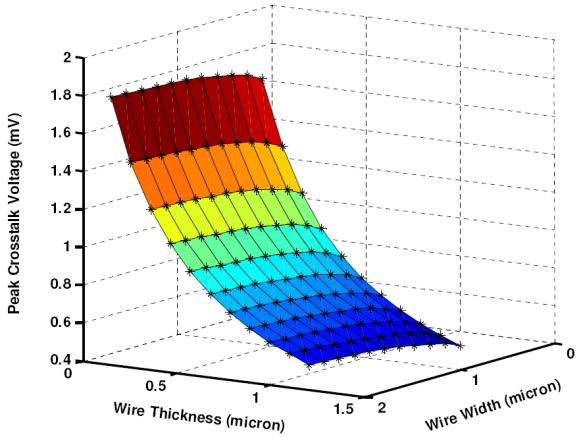

Figure 5. Crosstalk voltage as a function of a wire width and thickness.

studied over here. The study has been extended to realize the peak crosstalk voltage as shown in the following figure. In Figure 5 variation of peak crosstalk voltage has been revealed for the simultaneous variation of interconnect wire width and thickness. The voltage varies from 41 mV to 178 mV, here we had varied the wire width from 0 to 2 micron where as the wire thickness has been varied from 0 to 1.2 micron. A nonlinear decrease in the peak voltage has been realized with the increase in the wire thickness, almost negligible effect of wire width on the crosstalk voltage has been observed.

4. CONCLUSIONS

The interconnect layer capacitance significantly gets affected by the interwire spacing and the interconnect perimeter. The peak crosstalk time shows the non linear increase with propagation delay. The peak crosstalk voltage founds to be maximum for the lower values of the wire thickness, while the wire width does not affects much on the crosstalk voltage. The dimensions of the interconnect, the capacitance, crosstalk time and crosstalk voltage needs to be optimized for designing a better, high speed and less power consuming VLSI chips.

REFERENCES

1. Ma, H. and Q. Feng, "Design of a low power, high performance BICMOS current-limiting circuit for DC-DC converter application," *PIERS Online*, Vol. 3, 368, 2007.
2. Cao, Y., Q. J. Zhang, and I. Erdin, "Neural-based transient behavioral modeling of IC buffers for high-speed interconnect design," *PIERS Online*, Vol. 3, 1136, 2007.
3. Vasilopoulou, M., S. Tsevas, A. M. Douvas, P. Argitis, D. Davazoglou, and D. Kouvatstos, "Characterization of various low-k dielectrics for possible use in applications at temperatures below 160°C," *Journal of Physics: Conference Series*, Vol. 10, 218, 2005.
4. Ye, C., Z. Ning, Y. Xin, T. Wang, X. Yu, and M. Jiang, "Optical emission spectroscopy investigation on SiCOH films deposition using decamethylcyclopentasiloxane electron cyclotron resonance plasma," *Microelectronic Engineering*, Vol. 82, 35, 2005.
5. Wu, H.-I., Z. H. Hsiung, and C. F. Jou, "A 0.75 V CMOS low-noise amplifier for ultra wide-band wireless receiver," *PIERS Online*, Vol. 3, 976, 2007.
6. Rouessac, V., L. Favennec, B. Re´miat, V. Jousseaume, G. Passemard, and J. Durand, "Precursor chemistry for ULK CVD," *Microelectronic Engineering*, Vol. 82, 333, 2005.
7. Ryu, J. and S. Nam, "Very low power single-ended cross-coupled oscillator in CMOS technology," *PIERS Online*, Vol. 3, 1037, 2007.
8. Wu, H. I., R. S. Fan, and C. F. Jou, "A 0.7 V transformer-feedback CMOS low-noise amplifier for 5-GHz wireless LAN," *PIERS Online*, Vol. 3, 968, 2007.
9. Xiao, F. and Y. Kami, "Modeling and analysis of crosstalk between differential lines in high-speed interconnects," *PIERS Online*, Vol. 3, 1293, 2007.

10. Kirawanich, P., J. R. Wilson, N. E. Islam, and S. J. Yakura, "Minimizing crosstalks in unshielded twisted-pair cables by using electromagnetic topology techniques," *Progress In Electromagnetics Research*, PIER 63, 125, 2006.
11. Nagai, H., M. Hori, T. Goto, T. Fuji, and M. Hiramatsu, "Fabrication of multilayered SiOCH films with low dielectric constant employing layer-by-layer process of plasma enhanced chemical vapor deposition and oxidation," *Jpn. J. Appl. Phys.*, Vol. 42, 2775–2779, 2003.
12. Li, Y., S. Yue, Y. Zhao, and G. Liang, "Low power dissipation SEU-hardened CMOS latch," *PIERS Online*, Vol. 3, 1080, 2007.
13. Stallein, M., C. Kolleck, and G. Mrozynski, "Improved analysis of the coupling of optical waves into multimode waveguides using overlap integrals," *Progress In Electromagnetics Research Symposium*, 464, Hangzhou, China, 2005.
14. Viitanen, A. J., I. S. Nefedov, and S. A. Tretyakov, "Field propagation in nanoporous metal waveguides," *PIERS Online*, Vol. 3, 1080, 2007.
15. Kirawanich, P. and N. E. Islam, "An electromagnetic topology approach: Crosstalk characterization of the unshielded twisted-pair cable," *Progress In Electromagnetics Research*, PIER 58, 285, 2006.
16. Xiao, F., R. Hashimoto, K. Murano, and Y. Kami, "Analysis of crosstalk between single-ended and differential lines," *PIERS Online*, Vol. 3, 16, 2007.
17. Wu, W.-L., W. E. Wallace, E. K. Lin, G. W. Lynn, C. J. Glinka, E. T. Ryan, and H.-M. Ho, "Properties of nanoporous silica thin films determined by high-resolution x-ray reflectivity and small-angle neutron scattering," *J. Appl. Phys.*, Vol. 87, No. 3, 1193, 2000.
18. Rouquerol, J., D. Avnir, C. W. Fairbridge, D. H. Everett, J. H. Haynes, N. Pernicone, J. D. F. Ramsay, K. S. W. Sing, and K. K. Unger, "Recommendations for the characterization of porous solids," *Pure and Appl. Chem.*, Vol. 66, 1739, 1994.
19. Tripathi, R., R. Gangwar, and N. Singh, "Reduction of crosstalk in wavelength division multiplexed fiber optic communication systems," *Progress In Electromagnetics Research*, PIER 77, 367, 2007.
20. Morgen, M., E. T. Ryan, J.-H. Zhao, C. Hu, T. Cho, and P. S. Ho, "Low dielectric constant materials for ULSI interconnects," *Annu. Rev. Mater. Sci.*, Vol. 30, 645, 2000.