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A COMPACT 2.4/5.2-GHZ RAT-RACE COUPLER ON GLASS SUBSTRATE

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Abstract—This paper presents the design and implementation of a compact 2.4/5.2-GHz rat-race coupler on a glass substrate. Due to the low-loss substrate and thick metal layers, the process provides high-Q capacitors and inductors, and therefore the lumped rat-race coupler is practical. The coupler consists of three bandpass and one bandstop networks to achieve dual-band operations. The measured insertion losses at 2.4 GHz and 5.2 GHz are less than 2.7 dB and 1.9 dB. The measured return losses at the frequencies of interest are better than 20 dB. Moreover, the phase imbalances at the in-phase and anti-phase output ports are less than 3.9° and 4° at 2.4 GHz and 5.2 GHz, respectively. The chip size including all testing pads is merely $2.87 \times 2.1\,\text{mm}^2$ which is comparable to on-chip levels.

1. INTRODUCTION

Rat-race couplers are widely used in the radio-frequency (RF) front-end of communication systems for equal power splitting with in-phase and anti-phase responses at different output ports. Recently, many dual-band rat-race couplers are reported for facilitating the system integration and simplifying the architecture of the RF front-end [1–6]. The conventional transmission line (TL)-based works modify electrical length, characteristic impedance, and open/short stubs of their TLs for circuit miniaturization [1–3]. Moreover, other rat-race couplers incorporating composite right/left-handed (CRLH) TLs or lumped resonators also demonstrate their feasibility and further size reduction successfully [4–6]. However, these conventional and artificial TL-based couplers on the printed-circuit board (PCB) still occupy large chip

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area compared to on-chip circuits, and thus increase the cost and incur additional power consumption of packaging.

CMOS technologies feature low-cost manufacturing and high-volume integrating capabilities, and rapid developments of wireless communications make systems on a single chip (SOC) practical [7, 8]. However, frequency-scaling and TL-based couplers or filters do not benefit from the accelerated process scaling of CMOS technologies. Therefore most of on-chip distributed circuits are implemented at millimeter-wave frequencies for the chip area and insertion loss considerations [9–11]. Moreover, quality (Q) factors of CMOS inductors suffering from its low-resistivity substrate are around 10, which limits lumped designs by LC components at microwave frequencies. Many high-Q inductor techniques such as silicon-on-insulator (SOI) or micro-electro-mechanical system (MEMS) are proposed to minimize resistive losses in the P-type substrate [12–14]. The peak-Q factors of these inductors in the CMOS-compatible process range between 20 and 30 which are successfully applied to an LC filter or voltage-controlled oscillator (VCO) design. Typically, acceptable performances of passive circuits require inductors with Q-factor of 30 at least.

In this paper, a lumped 2.4/5.2-GHz rat-race coupler in a CMOS-compatible process is presented for wireless local area network (WLAN) applications. The process provides a low-loss glass substrate to reduce substrate losses, three thick metal layers to reduce conductor losses, and bumpers to integrate CMOS RFICs in a flip-chip form as shown in Figure 1. High-Q factors of inductors and capacitors of the process are achievable, and are applied to the proposed LC-

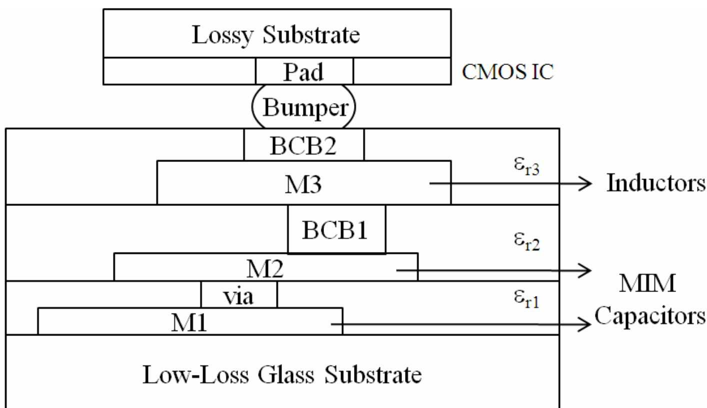

Figure 1. Cross-section view of the glass substrate process.

based coupler which demonstrates the feasibility of lumped-element based designs on this glass substrate. The coupler consists of three bandpass and one bandstop networks to achieve dual-band operations. The organization of this paper is as follows. In Section 2, the design of the lumped coupler and LC components on the glass substrate will be presented. Section 3 discusses the experimental results and the pad layout of the coupler. Finally, Section 4 concludes this work.

2. DESIGN OF LUMPED-ELEMENT BASED COUPLERS

2.1. Lumped Dual-band Coupler

Conventional TL-based couplers consume too much chip area, and therefore lumped-element topologies including Π-network or T-network have been proposed to realize compact couplers [15–17]. Typically, a single-band rat-race coupler consists of three $\lambda/4$ TLs and one $3\lambda/4$ TL which can be also replaced by three lowpass and one highpass networks, respectively. The proposed rat-race coupler is composed of three bandpass and one bandstop networks to achieve dual-band operations as shown in Figure 2. The bandpass network represents a $3\lambda/4$ TL at the low frequency (f_1), and a $\lambda/4$ TL at the high frequency (f_2). On the contrary, the bandstop network represents a $\lambda/4$ TL at f_1, and a $3\lambda/4$ TL at f_2. Consequently, a dual-band rat-race is achievable by these bandpass and bandstop networks. Based on the ABCD matrices of TLs and the lumped-element networks, the lumped LC components can be obtained by equating the matrices as shown in Equations (1)–(2).

$$\begin{bmatrix} 0 & -jZ_0 \\ -jY_0 & 0 \end{bmatrix} = \begin{bmatrix} 1-BX & jX \\ j(2B-B^2X) & 1-BX \end{bmatrix}, \text{ for a } 3\lambda/4 \text{ TL} \quad (1)$$

$$\begin{bmatrix} 0 & jZ_0 \\ jY_0 & 0 \end{bmatrix} = \begin{bmatrix} 1-BX & jX \\ j(2B-B^2X) & 1-BX \end{bmatrix}, \text{ for a } \lambda/4 \text{ TL} \quad (2)$$

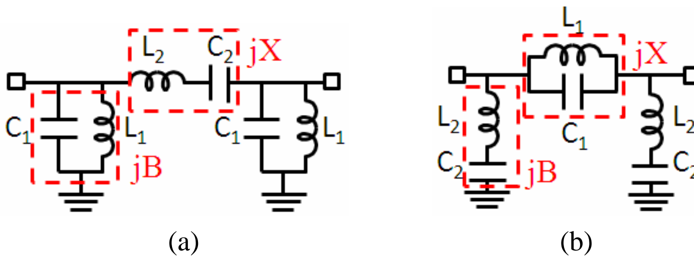

Figure 2. (a) Bandpass network. (b) Bandstop network.

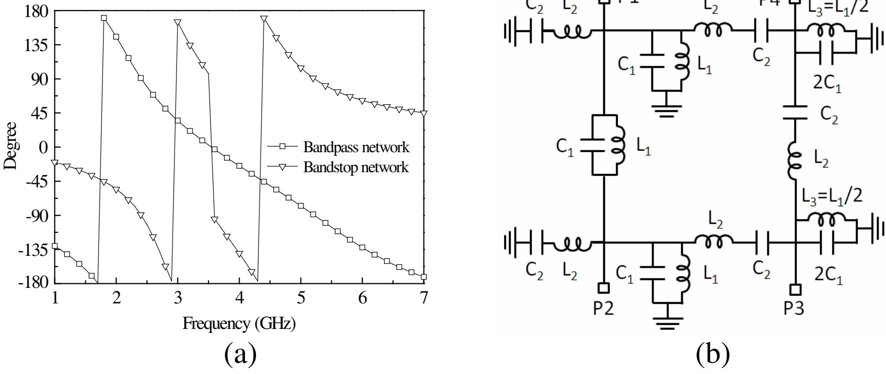

Figure 3. (a) Simulated electrical length of the bandpass and bandstop networks. (b) Schematic of the dual-band rat-race coupler.

where Z_o is the characteristic impedance of TLs. In this design, Z_o, f_1, and f_2 are 70.7 Ω, 2.4 GHz, 5.2 GHz, respectively. And the corresponding values of components can be derived from Equations (3)–(6). Therefore L_1, L_2, C_1, and C_2 are 2.535 nH, 4.036 nH, 0.801 pF, and 0.503 pF, respectively. Figure 3(a) shows simulated electrical length of the bandpass and bandstop networks. The electrical length of the bandpass network is 90° and −90° at 2.4 GHz and 5.2 GHz, respectively. And the electrical length of the bandstop network is −90° and 90° at 2.4 GHz and 5.2 GHz, respectively. The results verify the proposed lumped rat-race coupler mentioned above, and Figure 3(b) shows the complete schematic of the coupler.

$$L_1 = \frac{f_2 - f_1}{2\pi f_2 f_1} Z_o \quad (3)$$

$$C_1 = \frac{1}{2\pi (f_2 - f_1) Z_o} \quad (4)$$

$$L_2 = \frac{Z_o}{2\pi (f_2 - f_1)} \quad (5)$$

$$C_2 = \frac{f_2 - f_1}{2\pi f_2 f_1 Z_o} \quad (6)$$

2.2. Capacitors and Inductors on the Glass Substrate

The low-loss glass substrate with three metal layers (M1–M3) is shown in Figure 1. Popular CMOS RFICs can be integrated into the glass

substrate by bumpers and bonding pads in a flip-chip form. Due to the thick metal layers ($\geqq 3\,\mu\text{m}$) and low-loss glass substrate ($\tan\delta = 0.003$), the process provides high-Q (peak-$Q > 20$) inductors which are impractical in a standard CMOS process. Capacitors of the proposed process are realized by metal-insulator-metal (MIM) capacitors, and the two parallel-plate layers use M1 and M2 layers because of the ultra-thin and high-k dielectric layer. The dielectric constant (ε_{r1}) and thickness (d) of the dielectric is 7.0 and 0.2 μm, respectively. Therefore the corresponding capacitance (C_{mim}) and the capacitance density (C_{min}/A) of the capacitors can be obtained by the following equations.

$$C_{\text{mim}} = \varepsilon_r \varepsilon_o \frac{A}{d} \tag{7}$$

$$\frac{C_{\text{mim}}}{A} = \frac{\varepsilon_r \varepsilon_o}{d} \simeq 0.31\,\text{fF}/\mu\text{m}^2 \tag{8}$$

where A is the overlap area between M1 and M2, and the thicknesses of M1 and M2 are both 3 μm. Compared to a standard CMOS process with a capacitance density of $1\,\text{fF}/\mu\text{m}^2$, the proposed process features inferior capacitance density but good Q factors.

Low-Q CMOS inductors degraded by the lossy P-type substrate and thin metal layers limit their applications such as LC-based filters and couplers at low frequencies. All inductors are implemented on the top metal layer (M3) with a thickness of 12 μm for high-Q factors. The thick metal layer (M3) reduces the resistive losses, and the low-loss glass-substrate reduces the substrate losses. Therefore high-Q inductors on the glass substrate are practical. Layouts of the MIM capacitors (C_1 and C_2) are square for the process variation considerations, and the simulated Q factors of the capacitors are greater than 94 from 2.4 GHz to 5.2 GHz shown in Figure 4(a). The minimum line-width and spacing on M3 layer which are required by the photolithography are both 10 μm. Therefore the minimum spacing of the spiral inductors (L_1, L_2, and L_3) is chosen for compact layouts, and the line-width of 15 μm is designed for high-Q factors. The Q factors of the inductors range between 24 and 35 from 2.4 GHz to 5.2 GHz as shown in Figure 4(b). Typically, smaller inductors feature higher Q factors and self-resonance frequencies. Figure 4(c) shows the chip photo of C_1 and L_2. The chip area of C_1 and L_2 excluding testing pads are 130 μm ×160 μm and 480 μm ×500 μm, respectively. Moreover, the active area of L_1 and C_2 are 480 μm ×380 μm and 170 μm ×280 μm. C_2 is composed of two series capacitors, and therefore it consumes larger chip area than C_1. The compact sizes of these components are nearly comparable to on-chip levels. Good agreement between measured and simulated results demonstrates the feasibility of these superior

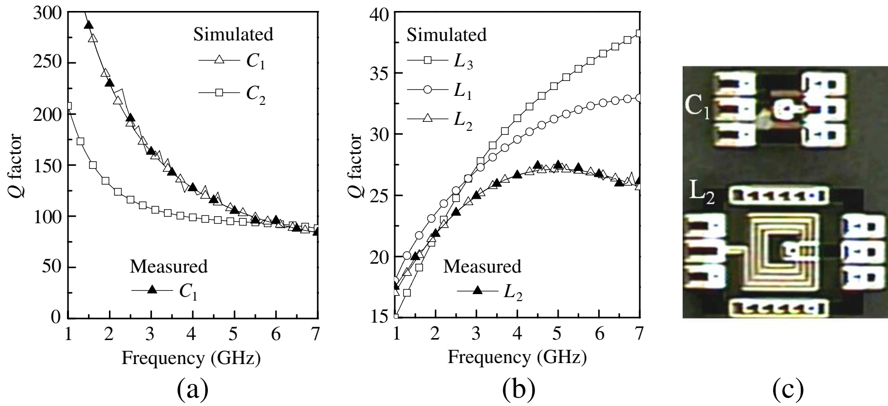

Figure 4. Simulated and measured Q factors of (a) capacitors and (b) inductors. (c) Chip photo of C_1 and L_2.

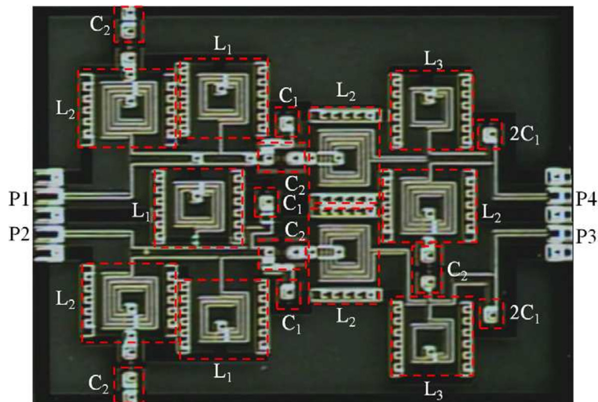

Figure 5. Chip photo of the coupler.

components on this glass substrate. In summary, it is convinced that these high-Q components are applicable to the lumped-element based coupler.

3. EXPERIMENTAL RESULTS AND DISCUSSION

Two face-to-face GSGSG RF probes with a pitch-to-pitch of 100 μm were used to characterize the four-port coupler as shown in Figure 5. The chip size including all testing pads is $2.87 \times 2.1\,\mathrm{mm}^2$ on the glass substrate which is approximately 200 μm thick. The ground plane of

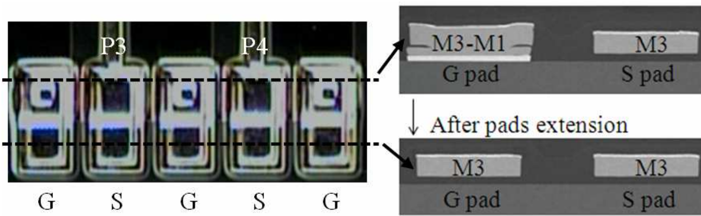

Figure 6. Pad extension for metal planarization considerations.

the coupler is defined at M1 layer, and therefore the ground (G) pads are realized from M1 to M3 layers which are connected by via, M2, and BCB1 layers. All MIM capacitors consist of M1 and M2 layers, and their M1 layers are placed at some isolated areas to avoid signals grounded. Moreover, the signal (S) pads are merely implemented on M3 layer. Figure 6 shows the vertical and cross-section chip photo of the GSGSG pads with P3 and P4, and each testing pad is 148 μm ×74 μm which is composed of two 74 μm ×74 μm squares. Due to the presence of via, M2, and BCB1 layers, central regions of the G pads (the first square close to the coupler) are sunken, and the heights of G pads and S pads are uneven. In order to achieve the metal planarization of testing pads, all the pads are extended by M3 layer (the second square for probing) as shown in Figure 6. Finally, the pad extension provides smooth and even metal layers for standard measurements by the coplanar waveguide (CPW) probes.

Four-port S-parameter experiments of the lumped coupler were performed by on-wafer measurements, and undesired parasitic of the pads and interconnections were removed by a de-embedding procedure. The simulated and measured results of S parameters and phase differences are plotted in Figure 7. Both simulated and experimental results agree well because of the accuracy in full-wave electromagnetic simulations including process variations such as thickness of dielectric and metal layers. The measured $|S_{41}|$ and $|S_{43}|$ is -5.7 dB and -5.3 dB at 2.4 GHz, respectively. And the measured $|S_{41}|$ and $|S_{43}|$ is -4.4 dB and -4.9 dB at 5.2 GHz, respectively. The measured return losses ($|S_{11}|$ and $|S_{44}|$) at the frequencies of interest are better than 20 dB. Phase differences at the in-phase output port are 3.9° and 1.3° at 2.4 GHz and 5.2 GHz, respectively. Moreover, phase differences at the anti-phase output port are 176° and 178° at 2.4 GHz and 5.2 GHz, respectively. The inductors feature higher Q factors at 5.2 GHz as shown in Figure 4(b), and therefore better electrical characteristics of the lumped coupler are obtained at 5.2 GHz.

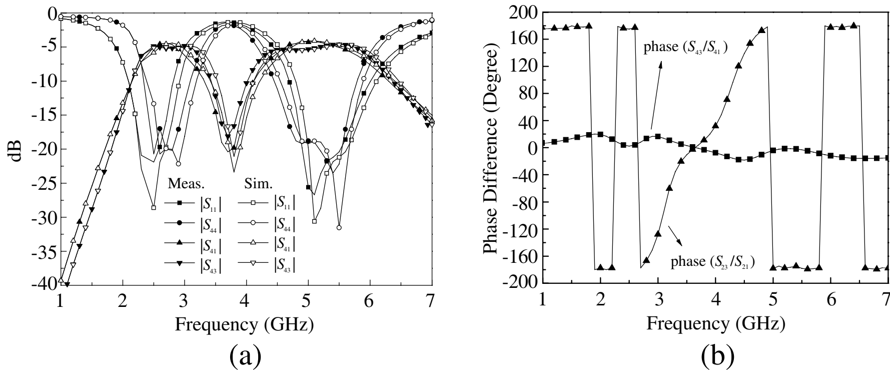

Figure 7. (a) Simulated and measured S parameters. (b) Measured phase differences.

4. CONCLUSION

In this paper, a compact 2.4/5.2-GHz rat-race coupler in a CMOS-compatible process is presented for WLAN applications. Due to the low-loss substrate and thick metal layers, the process provides high-Q capacitors and inductors which are impractical in a standard CMOS process. Moreover, popular CMOS RFICs can be integrated into the glass substrate by bumpers and bonding pads in a flip-chip form, and benefit these superior passive components. The lumped coupler using bandpass and bandstop networks to achieve dual-band operations is successfully designed, implemented and verified. Moreover, the layout of pads is also investigated for measurement considerations. Good electrical characteristics of compact the coupler clearly show the interest of the state-of-the-art process for the realization of several lumped circuits in microwave bands, such as filters, phase shifter, and matching network.

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