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A Novel Tunable Dual-Band Bandstop Filter (DBBSF) Using BST Capacitors and Tuning Diode

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Abstract—A novel approach to design Tunable Dual-Band Band-Stop filters will be presented in this paper. These filters have a new configuration with a coplanar microstrip line loaded with Stepped-Impedance Resonators (SIRs). These can be tuned by using tuning elements such as a tuning diode and ferroelectric capacitor. The Dual-Band Band-Stop Filter (DBBSF) and Dual-Band Band-Pass Filter (DBBPF) have become the most attractive circuit components in modern communication devices. Several studies have been done in this area but without tuning. Tuning is important in these circuits because the same circuit could be used in multiple band frequencies by applying a voltage, thus eliminating the need to design new circuits. This approach leads to smaller circuits with higher efficiency and reduced costs. The filters were designed with notch frequencies at 1.5 GHz and 3.5 GHz, and then loaded respectively with Tuning Diode or BST capacitors to compare their performances. The filter circuits were simulated with an Agilent ADS and Matlab program and were fabricated on FR-4 substrates. By loading the resonators with BST capacitors or tuning diodes, with no DC applied voltage, the first and second notch frequency shifts significantly. The application of DC bias to these varactors changes the center frequencies of the dual band filter.

1. INTRODUCTION

In recent years, tunable Dual Band Band-Pass Filters (DBBPFs) and Dual-Band Band-Stop Filters (DBBSFs) have become more attractive for scientists and researchers for their effectiveness in communication applications, with decreased size and cost. There are several approaches to designing tunable DBBPFs or DBBSFs by using tunable elements, such as p-n junction varactors, micro-electro mechanical systems (MEMS), liquid crystal cells and ferroelectric varactors. All of these tunable devices have been under investigation for the fabrication of tunable RF circuit blocks such as matching networks for power amplifiers voltage controlled oscillators, active and passive phase shifters and tunable antennas, as well as tunable filters

In [1–5], the researchers illustrate much research and many designs on this topic. In [1] they used stepped-impedance resonators (SIRs) to design DBBSFs. They used the second order of SIRs with four different values of impedances (Z) and electrical length (θ_l), but the filters were not tunable. Chin and Lung [2] used tri-section stepped-impedance resonators (TSSIRs) to design DBBSFs. They received good results for DBBSFs, but without any tuning. In [3], Wang et al. used a new technique called dual-plane defected structures to design DBBSFs. They tuned their design by changing the dimensions of the circuit elements. Fallahzadeh et al. [4] used split ring resonators (SRRs) to design a dual-band bandstop waveguide filter, and in [5] Abu Safia et al. designed a dual-band bandstop coplanar waveguide filter by using uniplanar series connected resonators. None of the previous research has addressed any tuning for DBBSFs' circuits by using tuning elements separately or independently for each band. One

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way to design DBBPFs is to combine two bandpass filters designed for different passbands. SIRs are widely used to design DBBPFs in dual-section or tri-section. Another method used to design DBBPFs is Microstrip Ring Resonators as shown in [8]. The design of DBBSFs at microwave frequency is still challenging since it has to take into consideration many parameters, including center frequency, bandwidth and voltage control.

In this paper, we use double transmission lines to design DBBSFs using a novel approach to connect two filters with each other to get dual-band frequencies, by loading tuning elements to tune each band separately or simultaneously by applying DC voltage on tuning elements.

2. THEORY AND DESIGN EQUATION OF DBBSFS

Microstrip Transmission Line Resonators (MTLRs) have been used widely to build many RF-Microwave circuits because of their features, such as easy fabrication, low cost, and small size. Double transmission lines in Fig. 1 have two impedances, Z_1 and Z_2, with each impedance having different electrical lengths of θ_1 and θ_2, respectively. In SIRs theory, the inductor will be implemented as high impedance ($Z_0 = Z_{high}$), and the capacitor will be implemented as low impedance ($Z_0 = Z_{low}$). The values of L_i and C_i can be determined by using the following equations:

$$L_i = \frac{1}{\omega_i g_i \Delta_i} \tag{1}$$

$$C_i = \frac{g_i \Delta_i}{\omega_i} \tag{2}$$

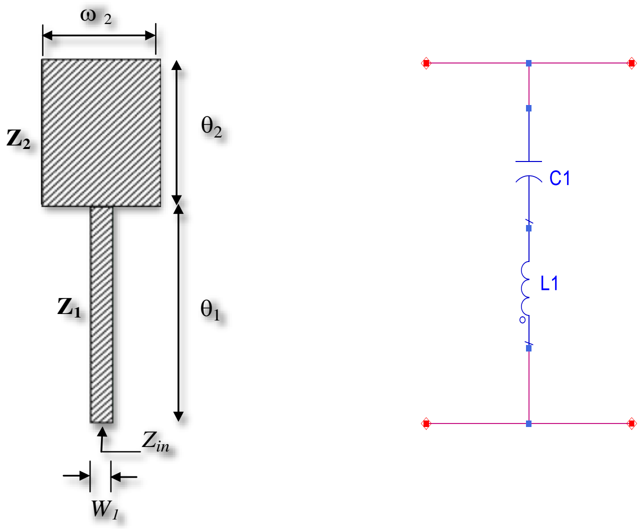
where g_i is the prototype element value, and Δ_i is the fractional bandwidth ($i = 1, 2, \ldots N + 1$).

The microstrip transmission line resonator shown in Fig. 1(a) has two input impedances. One is an open circuit line and the other a short circuit line, with the input impedance depicted by the following equation

$$Z_{in} = jZ_1 \frac{(Z_1 \tan\theta_1 - Z_2 \cot\theta_2)}{Z_1 + Z_2 \tan\theta_1 \cot\theta_2} \tag{3}$$

where θ_1 and θ_2 are the electric lengths of the microstrip.

$$R_Z = {}^{Z_h}\!/_{Z_l} = {}^{Z_1}\!/_{Z_2} = {}^{Y_2}\!/_{Y_1} \tag{4}$$



(a) (b)

Figure 1. Structure of double MTLR. (a) Two microstrip transmission line resonators. (b) Equivalence of series LC resonators.

where R_Z is the impedance ratio.

By assuming $Y_{in} = 0$ [6], R_Z yields

$$R_z = \frac{-1}{\tan\theta_1 \cot\theta_2} \tag{5}$$

In this design, the impedance ratio (R_z) should be as high as possible. The electric lengths for low impedance line (β_l) and high impedance line (β_h) sections can be determined by using the following equations [7]:

For low impedance lines:

$$\beta_l = \frac{g_k Z_l}{Z_0}, \quad k = 1, 3, 5, \ldots \tag{6}$$

For high impedance lines

$$\beta_h = \frac{g_k Z_0}{Z_h}, \quad k = 2, 4, 6, \ldots \tag{7}$$

g_k is the normalized element values of the low pass prototype, and these equations are valid when ($\beta_l < \pi/4$) [7]. One of the methods to design DBBSFs is to combine two filter circuits as shown in Fig. 2, in order to make each filter work in the specific frequency that we designed it to work in. This circuit will reject unwanted signals at the frequencies ω_1 and ω_2 that exhibit the response of a dual-band band-stop filter.

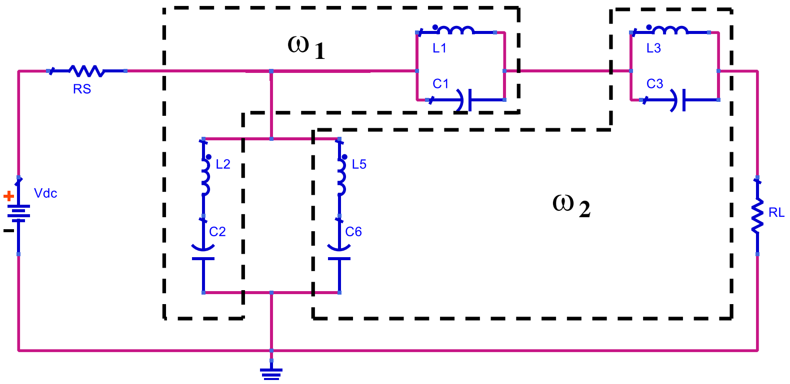


Figure 2. Lumped circuit of DBBSF.

In this study, we utilize two DBBSFs to work at two frequencies, 1.5 GHz and 3.5 GHz, by using two double MTLRs as shown in Fig. 3 [9] with two resonators for input and output ports with impedance $Z_0 = 5\,\Omega$. Using experimental results, Equations (6) and (7) can be modified to calculate the low and high impedance line sections for each transmission line, as follows.

For low impedance lines:

$$\beta_l = \frac{g_k Z_l}{2.75 \times Z_0}, \quad k = 1, 3, 5, \ldots \tag{8}$$

For high impedance lines

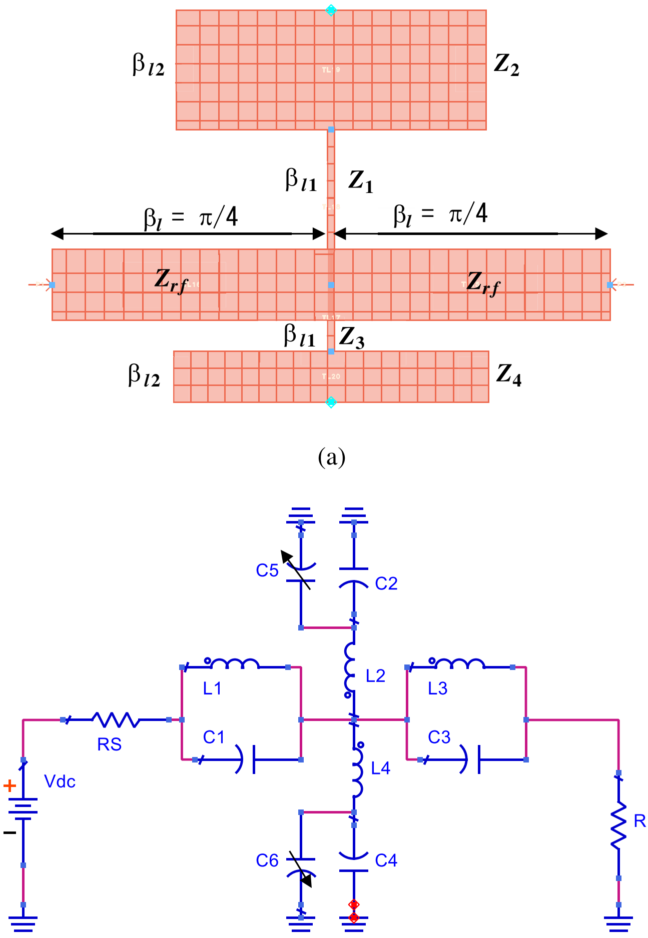
$$\beta_h = \frac{g_k Z_0}{2.75 \times Z_h}, \quad k = 2, 4, 6, \ldots \tag{9}$$

From Fig. 3(b) we can calculate both Z_1 and Z_2 impedances, and Z_{TOTAL} from the following equations [9]

$$Z_1 = j\omega_a L_a + \frac{1}{j\omega_a C_a} \tag{10}$$

$$Z_2 = j\omega_b L_b + \frac{1}{j\omega_b C_b} \tag{11}$$

$$Z_T = Z_1 // Z_2 = \frac{Z_1 Z_2}{Z_1 + Z_2} \tag{12}$$



(a)

(b)

Figure 3. (a) DBBSF circuit using two MTLRs. (b) Equivalent lumped circuit for two MTLRs.

$$\therefore Z_T = \frac{(j\omega_a\omega_b C_a C_b)\left(-\omega_a^2\omega_b^2 L_a L_b C_a C_b + \omega_a^2 L_a C_a + \omega_b^2 L_b C_b - 1\right)}{(\omega_a\omega_b C_a C_b)\left(-\omega_a^2\omega_b L_a C_a C_b - \omega_b^2\omega_a L_b C_a C_b + \omega_a C_a + \omega_b C_b\right)} \tag{13}$$

ω_a is the first band frequency, ω_b the second band frequency, and $L_a L_b$ are the inductors $L_2 L_4$. C_a is the total capacitor of the first filter $C_a = C_1//C_5$, and C_b is the total capacitor of the second filter $C_b = C_4//C_6$. The capacitors C_5 and C_6 are the equivalent capacitors of the tuning diode or ferroelectric capacitor with variable values as depicted in Fig. 3(b).

We utilize the Butterworth method with $N = 3$ to find the element values for the low pass prototype to use in Equations (1) and (2), and by using Advanced Design System software (ADS), we can get the width (W) and length (L) for each microstrip impedance. The dimension of impedance Z_{rf} in Fig. 3(a) can be found from $\beta_l = \pi/4$ and ω_{rf}, where ω_{rf} is the frequency ratio among ω_1 and ω_2, which equals 2.5 GHz.

From Equations (1) and (2), we find the values of inductor L_2 and capacitor $C2$ ($L_2 = 26.53$ nH, $C_2 = 0.42$ pF) for the first filter to work at 1.5 GHz, and for the second filter to work at 3.5 GHz which are equal to $L_4 = 11.37$ nH and $C_4 = 0.18$ pf, as shown in Fig. 3(b). The values of the capacitors C_2 and C_4 are variables when we connect the tuning elements

3. CALCULATION AND SIMULATION OF S-PARAMETERS BY USING THE ADS AND MATLAB MODEL CIRCUIT

3.1. Modeling by Using Matlab

S_{11} and S_{21} are defined as Return Loss (RL) and Insertion Loss (IL). When RL has a higher value it causes less reflection, and the load is harmonically matched as defined by the following equation [7]:

$$RL - 20\log\left({}^{P_r}/_{P_{in}}\right)(\text{dB}) \tag{14}$$

P_r is the power reflected from the input source and P_{in} the input power (source).

$$\therefore RL = -20\log(\Gamma)(\text{dB}) \tag{15}$$

Γ is the voltage reflection coefficient.

The insertion loss should be as low as possible and is defined by the following equation [7]:

$$IL = -20\log\left({}^{P_l}/_{P_{in}}\right)(\text{dB}) \tag{16}$$

P_l is the load power and P_{in} the input power (source).

$$IL = -20\log(T)\,\text{dB} \tag{17}$$

From the S matrix [7], the determination of S_{11} and S_{21} is made by using the following general equation:

$$S_{ij} = \left.\frac{V_i^-}{V_j^+}\right|_{V_k^+=0 \text{ for } k\neq j} \tag{18}$$

S_{11} and S_{21} can be calculated for one branch of this filter in Fig. 3, and by using the same equations for another branch of the filter, S_{11} and S_{21} can be found.

From Equation (18), S_{11} will be determined as follows [10]

$$Z_L = Z_0 + \left({}^{1}/_{Y}//Z_0\right) \tag{19}$$

Substituting for Z_L in S_{11}, the yield is

$$S_{11} = -Z_0Y + (2 + YZ_0) \tag{20}$$

where Y is the admittance which equals

$$Y = \frac{1}{Z_1} \quad or \quad \frac{1}{Z_2} \tag{21}$$

We can calculate Z_1 and Z_2 impedances by using Equations (11) and (12).

S_{21} can be found by applying a source voltage E_1 to port 1, as follows [10]

$$I = \frac{E_1}{(Z_L + Z_0)} \tag{22a}$$

$$V_2 = V_2^- = \left({}^{1}/_{Y}//Z_0\right) I \tag{22b}$$

$$\begin{aligned} V_1 &= V_1^+ + V_1^- = V_1^+(1 + S_{11}) = Z_L I \Longrightarrow \\ V_1^+ &= Z_L I/(1 + S_{11}) \end{aligned} \tag{22c}$$

Dividing Equation (22b) by (22c), the yield is

$$S_{21} = V_2^-/V_1^+ = \left({}^{1}/_{Y}//Z_0\right)(1 + S_{11})/Z_L \tag{22d}$$

$$\therefore S_{21} = 2/(2 + YZ_0) \tag{23}$$

By computing the values of lumped elements L_2, C_2, L_4 and C_4 as shown in Fig. 3 using MATLAB program, the variation of scattering parameters with frequency for DBBS filter is shown in Fig. 4.

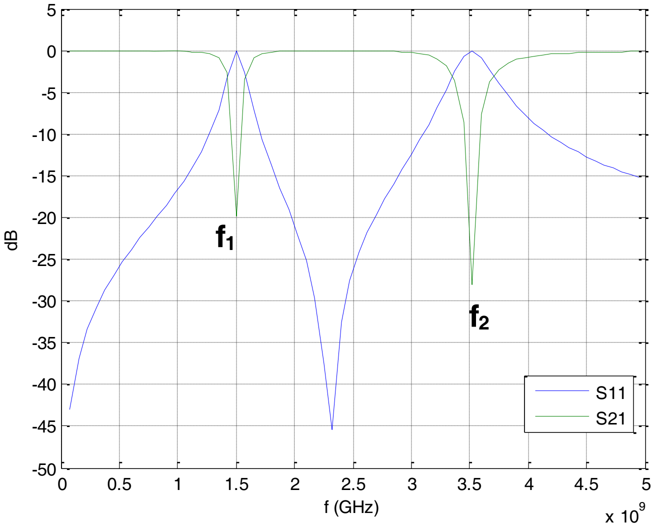


Figure 4. Variation of S_{11} and S_{21} with frequency of DBBSF by using MATLAB without tuning.

3.2. Simulation of S-Parameters By Using ADS

Figure 5 shows a circuit that we designed in ADS using the values of lumped components found from Fig. 3. The width and length for each lumped component are obtained from ADS. The simulation results in return loss (S_{11}) and insertion loss (S_{21}) of this circuit are shown in Fig. 6.

The simulation results from the two methods used to design this filter, viz: Matlab and ADS, show a good agreement between them, as shown in Figs. 4 and 6.

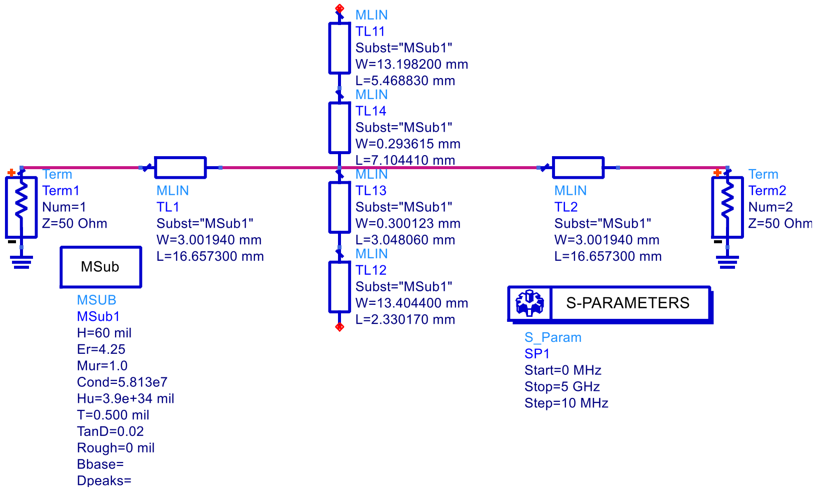


Figure 5. Dual band band-stop filter circuit used in ADS simulation.

4. DESIGN OF TUNABLE DBBSF

The tunable filters using p-n diode and ferroelectric capacitor were fabricated on an FR4 substrate with dielectric substrate of thickness 60 mils and loss tangent 0.002. The copper metallization has conductivity of 5.813×10^7 (ohm.cm^{-1}) and thickness 0.50 mils.

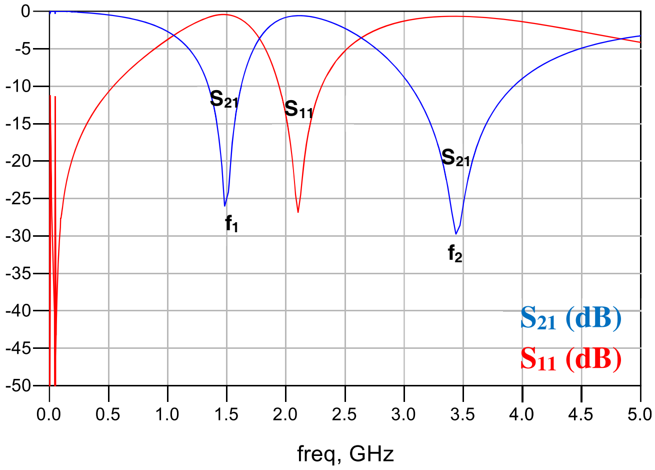


Figure 6. Simulated variations of S_{11} and S_{21}.

4.1. Design of Tunable DBBSF by Using Tuning Diode

Figure 7 shows the fabricated filter on the FR-4 substrate. Initially, a tuning diode (ZC390) was used to load the low frequency resonator (first branch) to tune this circuit. The capacitance of this tuning diode (ZC930) changes from about 10 PF to 1.5 PF by applying a voltage from 0 V to 5 V. The measured variations in S_{11} and S_{21} frequency with a tuning voltage of 0 V to 5 V are shown in Fig. 8.

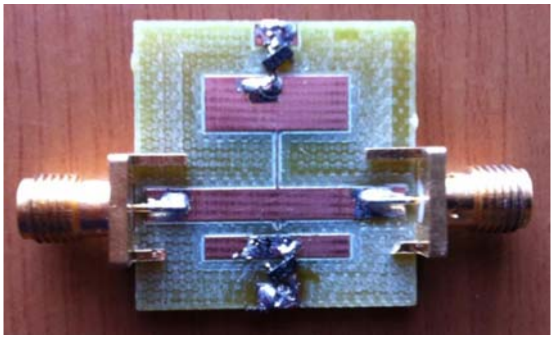


Figure 7. Fabricated DBBSF with tuning diode circuit.

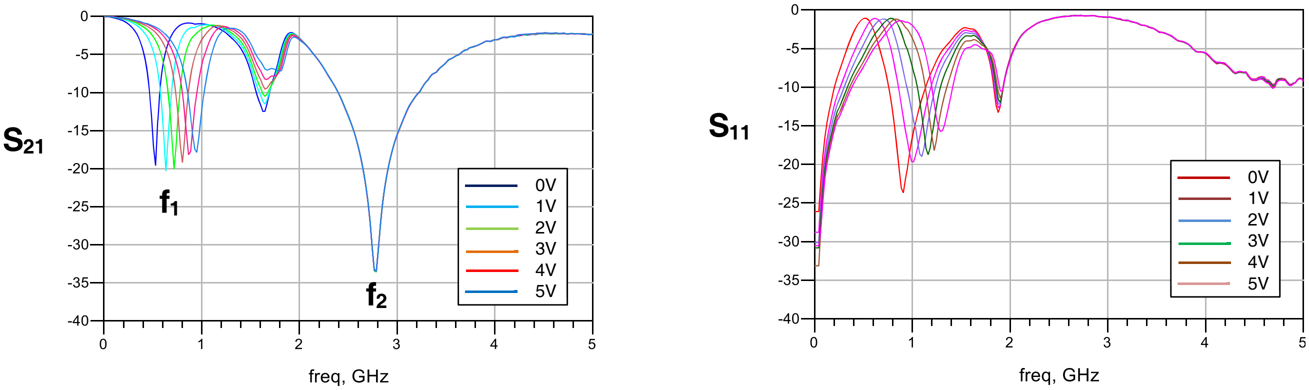


Figure 8. Measured variations of S_{11} and S_{21} for the first band stop filters tuned with p-n junction varactor reverse biased from 0 to 5 V.

The notch frequency of the filter can be changed from 527.8 MHz to 950 MHz by the application of a tuning voltage of 5 V. The tuning range is equal to 422.2 MHz (28% tuning range), while the second band notch frequency will stay constant at 2.787 GHz, and the return loss at the notch frequency is about −1.325 dB. Fig. 8 also shows a weak stop band notch response around 1.8 GHz, and the reason for its presence is not clear and may be attributed to parasitics. On the other hand, when the high frequency resonator (second branch) was loaded with tuning diode and the tuning voltage of 0 V to 5 V was applied, the variations of S_{21} and S_{11} are shown in Fig. 9. The second notch frequency is changed from 1.837 GHz to 3.209 GHz. The tuning range for the second branch is higher than for the first branch for the same applied voltage. Fig. 10 shows the variation of S_{21} with frequency when both the branches are loaded with diode varactor with applied tuning voltage from 0 to 5 V. The notch frequency in both bands can be tuned by this approach [11].

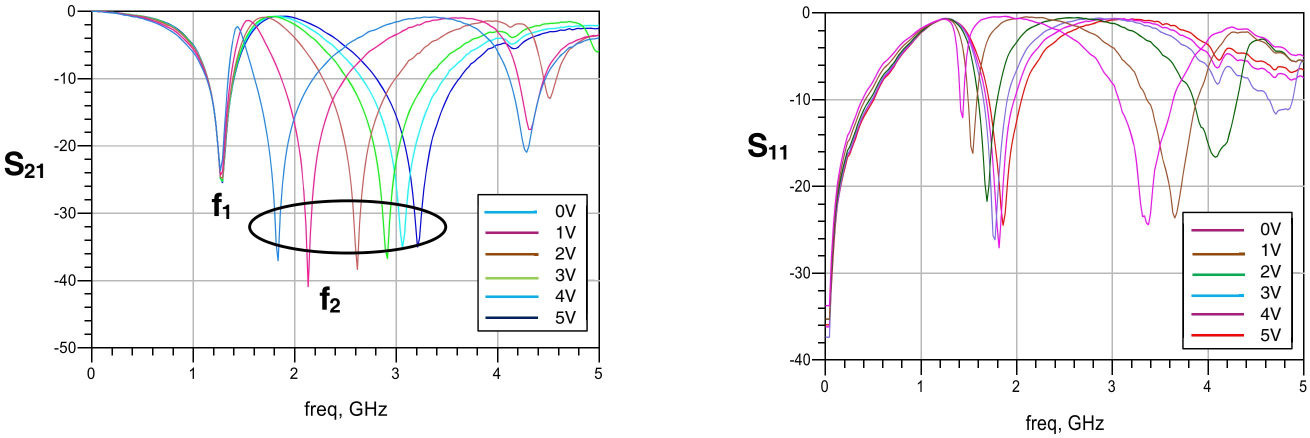


Figure 9. Measured variations of S_{11} and S_{21} for the second band stop filters tuned with p-n junction varactor 0–5 V.

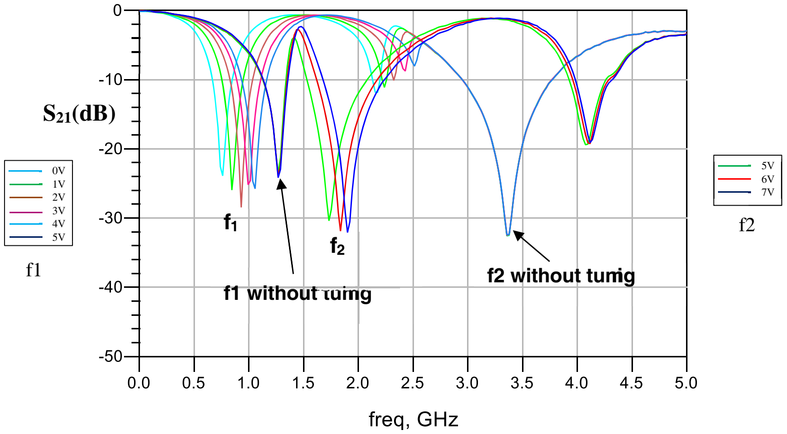
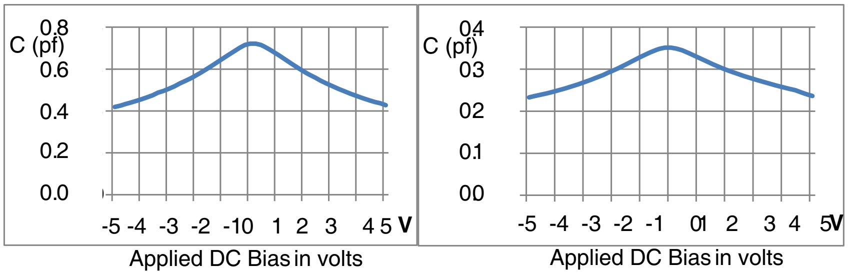


Figure 10. Measured variations of S_{21} for the DBBSF tuned with p-n junction varactor connected to both the branches.

4.2. Design of Tunable DBBSF by Using Ferroelectric BST Capacitor

Using the same circuit as before with the dimensions shown in Fig. 5, but instead of the tuning diode, ferroelectric varactors fabricated barium strontium titanate (BST), with capacitance versus characteristics as shown in Fig. 11(a) for low frequency resonator and (b) for high frequency resonators were used for tuning [9]. These varactors can be tuned with positive or negative bias voltages unlike tuning diodes which are tuned only in reverse bias mode.



(a) (b)

Figure 11. Capacitance versus voltage characteristics of a BST capacitor. (a) For low frequency (1.5 GHz), (b) For high frequency (3.5 GHz).

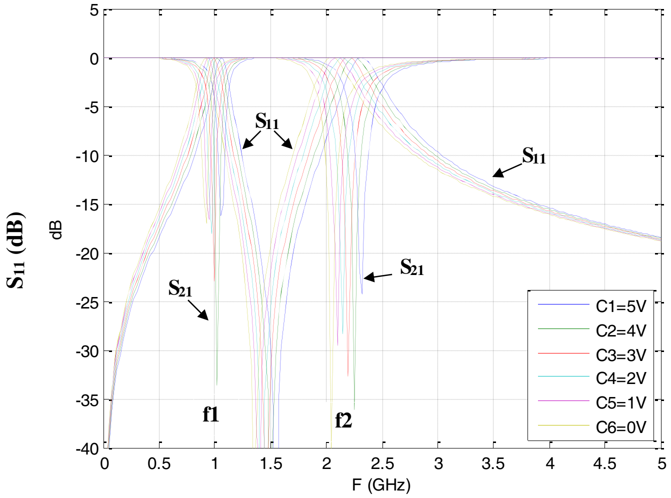


Figure 12. MATLAB simulation of S_{21} and S_{11} with frequency for DBBSF tuned with ferroelectric capacitor.

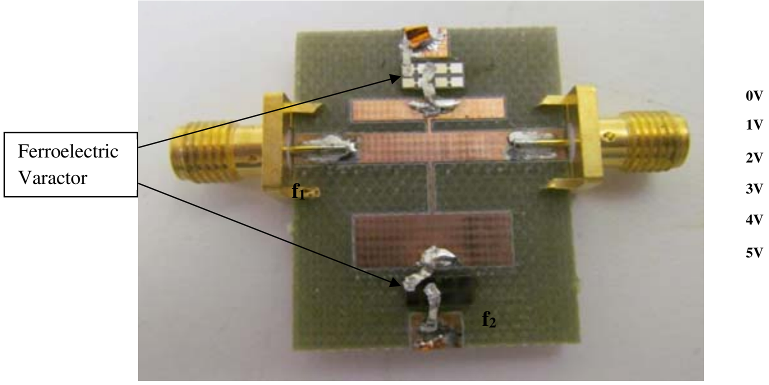


Figure 13. Fabricated DBBSF with BST varactor.

Figure 12 shows the MATLAB simulation of variation S_{11} and S_{12} with frequency for various applied voltages to ferroelectric varactors. The first branch of the filter can be tuned from 800 MHz to 1.15 GHz, whereas the second branch filter can be tuned from 2 GHz to 2.4 GHz. Ferroelectric varactors are electrically connected to an FR-4 board by using pressure bonding of indium ribbons. Fig. 13 shows the prototype of the filter fabricated on an FR-4 substrate with a BST tunable capacitor [11].

Figure 14 shows the measured variation of insertion loss for the tunable DBBSF with a single low frequency resonator loaded with FE capacitors [9]. The filter notch frequency can be tuned from 570 MHz to 781 MHz. The tuning range is equal to 211 MHz (14% tuning range). As expected, the second notch cannot be tuned, and it stays at 3.188 GHz. Fig. 15 shows the measured insertion loss for DBBSF when both resonators are loaded with FE capacitors. The first and second bands can be tuned. The first notch can be tuned from 565 MHz to 737 MHz, and the second notch can be tuned from 2.207 GHz to 2.55 GHz. The frequency tuning ranges for the first and second notches are 172 MHz (23.3% tuning range) and 343 MHZ (3.4% tuning range), respectively [11].

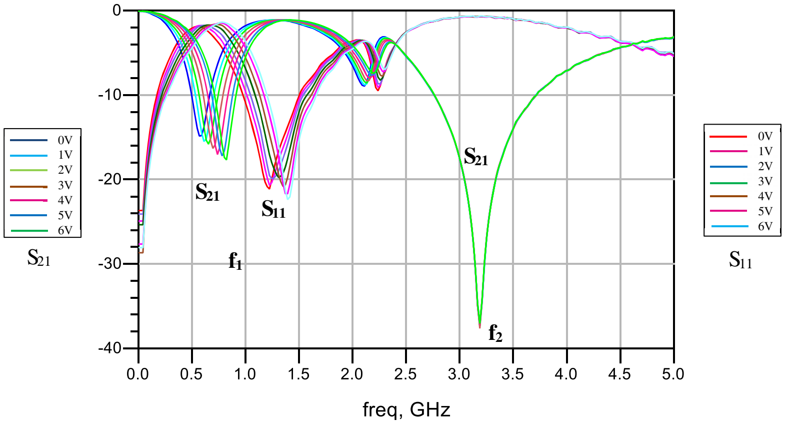


Figure 14. Variation of S_{21} and S_{11} with tuning voltage by loading one resonator with FE capacitor.

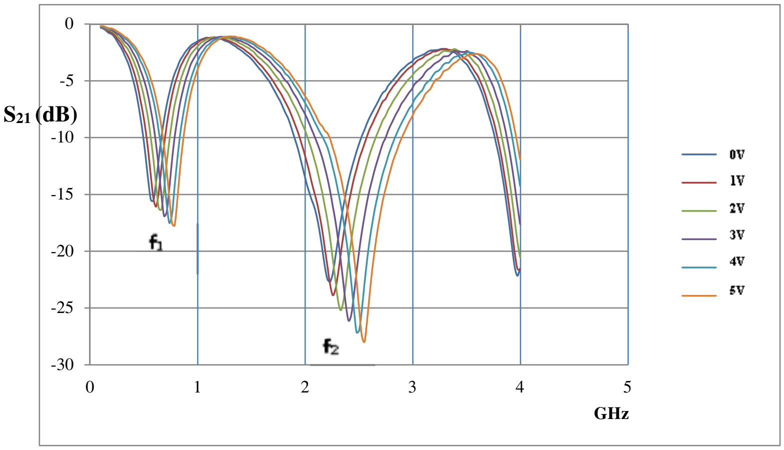


Figure 15. Variation of S_{21} with bias voltage by two resonators loaded with two FE capacitors.

5. CONCLUSION

Tuning DBBSFs are implemented with stepped impedance resonators loaded with tuning diode and ferroelectric BST capacitors. The frequency response of the filters can be controlled by the applied bias to the tuning elements. Measured response shows that the first notch frequency can be tuned from 1.098 GHz to 760 MHz when loaded with the tuning diode, and from 781 MHz to 570 MHz when loaded with the BST capacitors. The second notch frequency can be tuned from 3.336 GHz to 1.647 GHz when loaded from tuning diode, and from 2.55 GHz to 2.16 GHz when loaded with BST capacitors.

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