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STUDY OF THE INTER-STAGE CAPACITOR EFFECTS OF A RF CMOS POWER AMPLIFIER TO ENHANCE ITS EFFICIENCY

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Abstract—In this work, we analyze the effects of an inter-stage capacitor located between the power stage input and the driver stage output on the overall efficiency of a RF CMOS power amplifier and on gate-drain reliability problems. To verify the analyzed effects, we designed a RF CMOS power amplifier with a center frequency of 1.85-GHz. Class-D amplifiers with a feedback resistor are used as driver stages, and a class-E amplifier is used as the power stage. A distributed active transformer is adapted for use in the output power combiner for high efficiency. The inter-stage capacitor between driver and the power stage is removed to enhance the switching operation of the power stage. By eliminating the inter-stage capacitor, the supply voltage of the driver stage can be decreased compared to that in a general amplifier. Accordingly, the power-added efficiency is improved and the gate-drain reliability problems are moderated compared to a general amplifier. The analyzed effect of the inter-stage capacitor is verified successfully using the measured results of the designed amplifiers.

1. INTRODUCTION

Recently, the possibility of the RF CMOS power amplifier has been demonstrated successfully in various works [1–5]. The CMOS power amplifier can reduce the overall cost of a mobile system because the CMOS power amplifier can be integrated with other digital and analog circuits. However, the low efficiency of the CMOS power amplifier compared to a power amplifier using a compound semiconductor

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requires continuous research with the goal of improving the efficiency. Many previous works related to RF CMOS power amplifiers focused on a reduction of the loss induced by passive devices to increase the overall efficiency. In particular, the distributed active transformer is one of the most effective methods for reducing the loss induced by the output matching network [6–8]. A differential line inductor was introduced to enhance the efficiency in an inter-stage matching network [9]. CMOS power amplifier topologies have also been studied to obtain high efficiency. For example, numerous multi-mode power amplifiers have been introduced [8].

In this study, we analyze the effect of the supply voltage of the driver stage on the overall efficiency. An amplifier is designed for the mobile applications using the RF CMOS process.

2. EFFECTS OF A DC-BLOCKING CAPACITOR ON A RF CMOS POWER AMPLIFIER

2.1. Typical RF CMOS Power Amplifier

A typical power amplifier is designed using a multi-stage structure to obtain the required gain and output power, as shown in Figure 1. The driver stage of the power amplifier drives a power stage for a high overall gain of the amplifier. The role of the power stage is to generate watt-level output power to meet the output power specifications of the overall amplifier. In general, the power amplifier based on the RF CMOS process is designed as a switching mode amplifier because the linearity of CMOS is worse than that of the HBT. Additionally, the CMOS process simply enables the use of complimentary devices, known as NMOS and PMOS devices. Accordingly, a class-D amplifier as a driver stage can be easily designed using NMOS and PMOS devices. One of the many advantages of a class-D amplifier is that the output voltage waveform is rectangular, which enhances the transistor of the power stage to operate as a switch. Additionally, the class-D driver stage can be designed to have a compact size, as a bulky integrated inductor is not required.

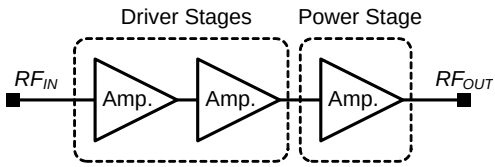

Figure 1. General power amplifier structure.

However, unlike the inverter used in the digital circuit, a class-D amplifier for a RF circuit applications requires a feedback resistor between the input and output nodes to compensate for the process variation of the PN ratio. Moreover, a feedback resistor in the class-D amplifier enhances the wide bandwidth characteristics. If class-D amplifiers as driver stages are designed with a cascade structure, a DC-blocking capacitor is generally inserted between each stage to isolate the feedback mechanism of each stage.

In general, the power stage of the switching-mode power amplifier is designed using class-E or class-F types so as to obtain watt-level output power [10]. In this work, we use the class-E type as the power stage. Additionally, the power stage is constructed using a cascade structure to solve the reliability problems arising from the drain-source breakdown voltage. A differential structure is adapted to solve the gain reduction problems induced by the parasitic inductance of the bonder-wires and feeding lines. In Figure 2, a simplified schematic of the general RF CMOS power amplifier topology is shown.

Figure 3 shows the voltage waveforms of the general RF CMOS

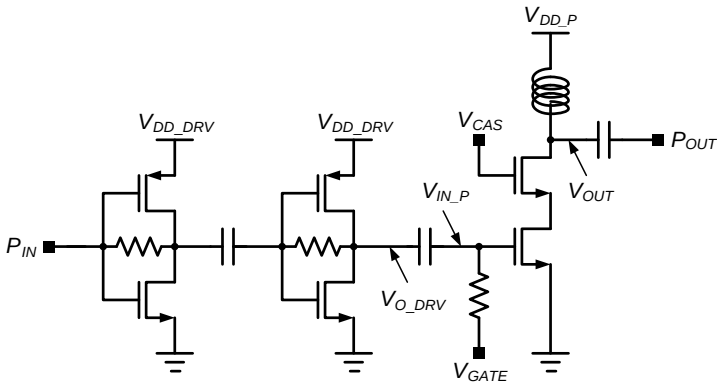

Figure 2. Simplified schematic of a general power amplifier.

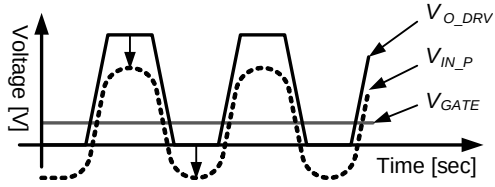

Figure 3. Voltage waveforms of the general RF CMOS power amplifier.

power amplifier shown in Figure 2. As shown in Figure 3, although the output voltage waveform of the class-D driver stage has a nearly rectangular form, the input voltage waveform of the power stage becomes almost sinusoidal-like owing to the DC-blocking capacitor located between the driver and the power stages. Additionally, the gate bias of the power stage is required to operate properly as a class-E amplifier, although an ideal class-E amplifier does not require additional gate bias. Moreover, the peak voltage value of the input voltage of the power stage is lower than that of the driver stage output.

2.2. RF CMOS Power Amplifier without an Inter-stage Capacitor

Figure 4 shows a simplified schematic diagram of the proposed power amplifier topology in which the inter-stage capacitor is removed. Accordingly, the input voltage waveform of the power stage is identical to the output voltage waveform of driver stage, as shown in Figure 5. Thus, the input voltage waveform of the power stage has nearly a

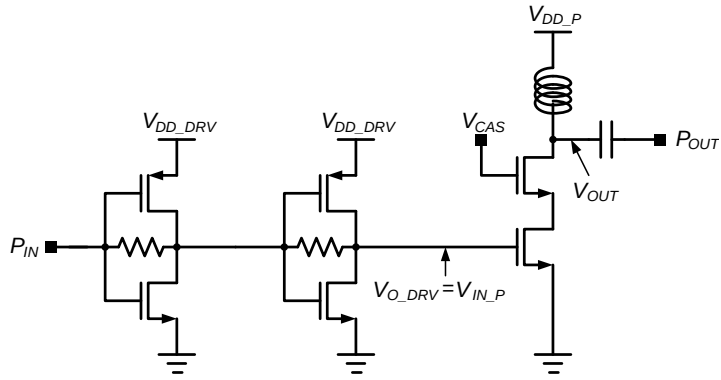

Figure 4. Simplified schematic of a power amplifier without an inter-stage capacitor.

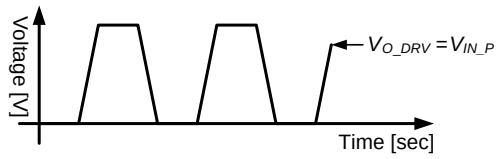

Figure 5. Voltage waveforms of a power amplifier without an inter-stage capacitor.

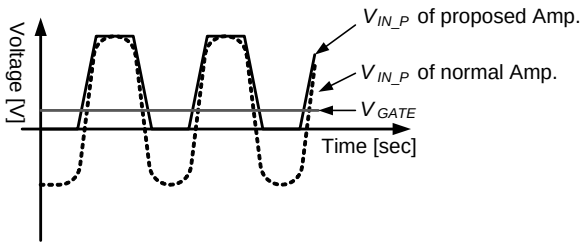

Figure 6. Comparison of the input voltage waveforms of the power stages.

rectangular form and the gate bias circuit of the power stage can be removed. The amplifier structure shown in Figure 4 can be operated in switching mode more easily compared to the general amplifier structure shown in Figure 2.

3. SUPPLY VOLTAGE EFFECTS ON RF CMOS POWER AMPLIFIER

As described in Section 2, the power stage input voltage shown in Figure 4 is higher than that shown in Figure 2 under the same supply voltage and input power conditions. Therefore, we can obtain the same peak voltage levels in Figure 2 and Figure 4, and the supply voltage of the driver stage in Figure 4 can decrease compared to that in Figure 2. With the lower supply voltage of the driver stage of Figure 4, the power stage input voltage waveforms can be redrawn, as shown in Figure 6.

Finally, the supply voltage of the driver stage without an inter-stage capacitor can be lower than that of the driver stage with an inter-stage capacitor. As the supply voltage of the driver stage is reduced, the power consumption at the driver stage decreases so as to increase the over power efficiency of the power amplifier. Generally, the efficiency of the power amplifier is calculated using power-added efficiency (PAE) as follows:

$$PAE = \frac{P_{OUT} - P_{IN}}{P_{DC}} \tag{1}$$

where P_{IN} is the input power, P_{OUT} is the output power, and P_{DC} is the overall DC power consumptions. We can decompose the P_{DC} into power consumptions in the driver-stage, P_{DRV} and in the power-stage, P_P, as follows:

$$PAE = \frac{P_{OUT} - P_{IN}}{P_{DC}} = \frac{P_{OUT} - P_{IN}}{P_{DRV} + P_P} \tag{2}$$

The power consumption in the driver-stage can be calculated as follows:

$$P_{DRV} \propto \frac{V_{DD\_DRV}^2}{R_{ON}} \tag{3}$$

where R_{ON} is the on-resistance of the driver-stage. From Eq. (3), we can compare the power consumptions for the normal amplifier and the proposed amplifier. As described above, the V_{DD_DRV} of the proposed amplifier is lower than that of the normal amplifier. For the sake of the simplicity, we assume that on-resistance is fixed according to the V_{DD_DRV}. Then, we can conclude that the power consumption in the driver stage of the normal amplifier, P_{DRV_nor} is higher than that of the proposed amplifier, P_{DRV_pro} as follows:

$$\frac{V_{DD\_DRV\_nor}^2}{R_{ON}} > \frac{V_{DD\_DRV\_pro}^2}{R_{ON}} \quad \text{and} \quad P_{DRV\_nor} > P_{DRV\_pro} \tag{4}$$

where $V_{DD\_DRV\_nor}$ is the supply voltage of the driver stage of the normal amplifier and $V_{DD\_DRV\_pro}$ is the supply voltage of the driver stage of the proposed amplifier. For example, if the $V_{DD\_DRV\_nor}$ is two times higher than the $V_{DD\_DRV\_pro}$, the P_{DRV_nor} is four times higher than the P_{DRV_pro}.

In this work, the designed supply voltage of the power stage is 3.3 V for mobile applications. A 1.65 V supply voltage is used for the driver stage for the proposed amplifier. The 1.65 V for input voltage of the power stage is enough for the switching mode operation of the power stage. However, for the normal power amplifier, the supply voltage of the driver stage is required to be 3.3 V to obtain a peak voltage of the input node of the power stage of 1.65 V. Therefore, the power consumption at the driver stage with an inter-stage capacitor is approximately two times higher than that of the amplifier without an inter-stage capacitor.

4. SUPPLY VOLTAGE EFFECTS ON RELIABILITY PROBLEMS

The existence of the inter-stage capacitor can affect the overall power efficiency of the power amplifier, as described in the previous sections. Additionally, the existence of the inter-stage capacitor can influence the reliability problems associated with the gate and drain voltages of the power stage MOSFET. Ideally, the phase of the drain is exactly opposite to that of the gate in a common-source amplifier structure. Thus, reliability problems always arise in the design of a watt-level RF power amplifier because the drain voltage can reach three times the supply voltage to obtain high power and good efficiency.

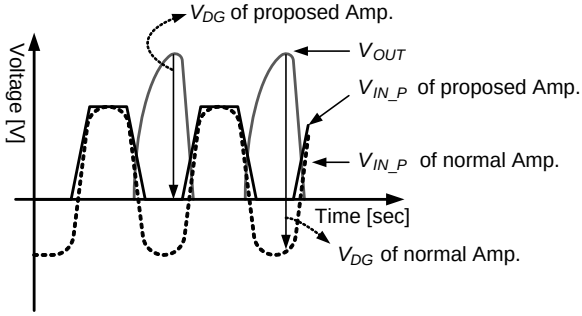

Figure 7. Gate and drain voltage waveforms of the power stage.

Figure 7 shows the gate and drain voltage waveforms of the power stage with and without an inter-stage capacitor. As described in Figure 7, the drain-gate voltage drop is nearly identical to the drain voltage for the amplifier without the inter-stage capacitor. However, the voltage drop is higher than the drain voltage for the amplifier with the inter-stage capacitor. If we design an amplifier under the conditions of 3.3 V supply voltage for the driver stage, 4 pF inter-stage capacitor, 1 pF parasitic capacitance for the gate of the power stage transistor, and 0.33 V gate bias voltage of the power stage, the peak value of the drain-gate voltage drop is approximately calculated as the drain voltage plus 1 V. The detailed calculation related to the drain-gate voltage drop can be described as Figure 8.

Thus, the reliability problems become more moderate in the power amplifier without the inter-stage capacitor compared with the amplifier with the inter-stage capacitor.

5. DESIGN OF THE POWER AMPLIFIER

Figure 9 shows a simplified schematic diagram of the proposed power amplifier with an inter-stage capacitor between the input node of the power stage and the output node of the driver stage. A distributed active transformer is used as a power combiner to obtain low load impedance for the power stage. The driver stages are designed using class-D amplifiers which are combined using a cascade connection. The DC-blocking capacitor between the driver stages is also removed to enhance the derivability of the first driver stage.

The power stage is designed using a cascade structure to improve the drain-source reliability. For the power transistors, MP1 has a total gate width of 2.048 mm and MP2 has a total gate width of 4.096 mm. The feedback resistor is 2.0 kΩ. The supply voltage for the power stage

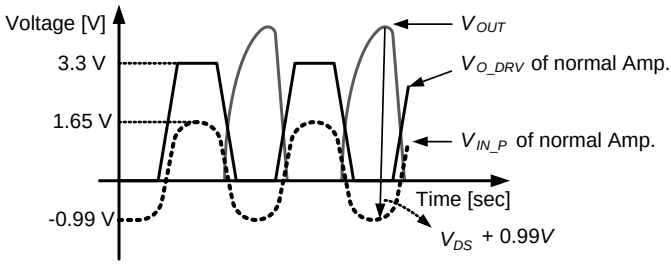

Figure 8. Gate and drain voltage waveforms of the power stage.

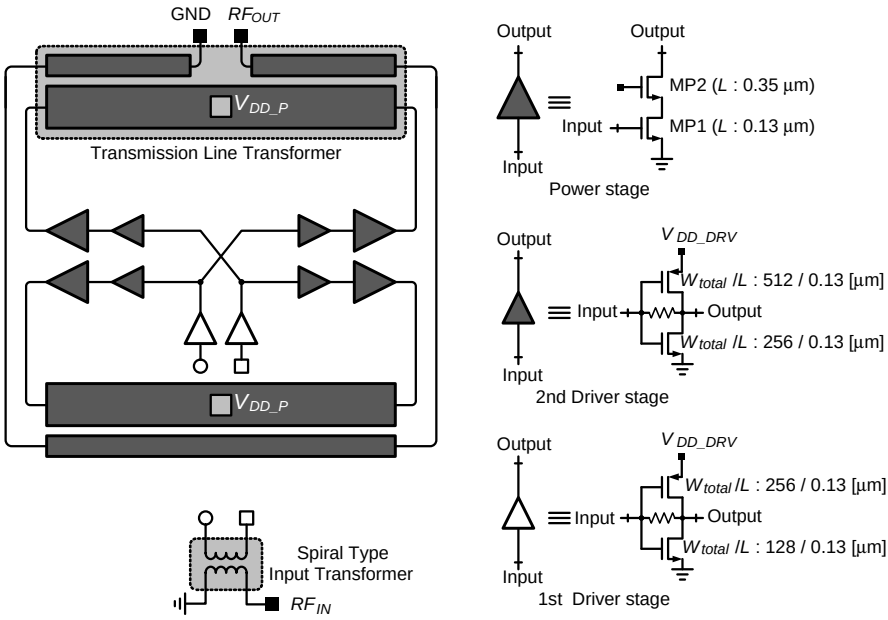

Figure 9. Schematic of the designed power amplifier.

is entered through virtual grounds located at the center of the primary parts of the output transformer. All of the matching components, including the output transformer, the input transformer, and the inter-stage matching network are integrated.

6. EXPERIMENTAL RESULTS

Figure 10 shows the implemented power amplifier using RF CMOS technology. The size of the chip is $1.7 \times 1.0\,\mathrm{mm}^2$ including the pads.

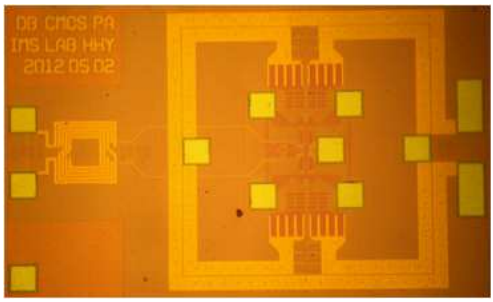

Figure 10. Photograph of the designed power amplifier (size: $1.7 \times 1.0\,\mathrm{mm}^2$).

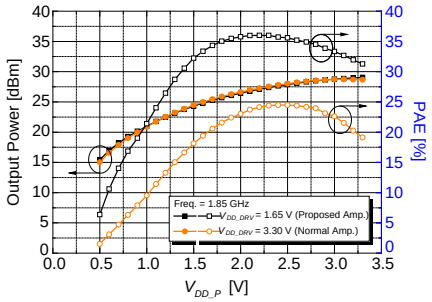

Figure 11. Measured output power and efficiency at an operating frequency of 1.85 GHz.

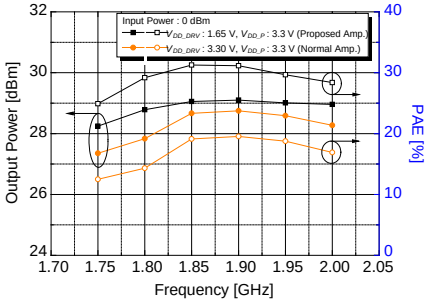

Figure 12. Measured frequency response under maximum output power conditions.

The area of the transformer is $1.0 \times 1.0\,\mathrm{mm}^2$.

Figure 11 shows the measured output power and power-added efficiency (PAE) of a general and the proposed power amplifier. The losses induced by the RF cable and the connectors for the measurement setup are de-embedded. However, the loss induced by the feeding lines in the printed circuit board and bonder-wires are included in the measured power and efficiency.

In this measurement, a 3.3 V supply voltage is used for the driver stage of the general amplifier, while the supply voltage is 1.65 V for the driver stage of the proposed amplifier. The supply voltage of the power stages of the general and proposed amplifiers varies from 0.5 V to 3.3 V. As shown in Figure 11, the measured output powers of the general and proposed amplifiers are nearly identical. On the other hand, the measured efficiency of the proposed amplifier is much higher than that of the general amplifier. At the maximum output power,

Table 1. Summary of the performance of fully-integrated CMOS power amplifiers.

Ref.	Center freq. [GHz]	P_{OUT} [dBm]	PAE [%]	Process [nm]	Size [mm]
[11]	2.4	23.4	31	180	1.0 × 1.7
[12]	2.4	30.1	33	90	2.06 × 2.1
[13]	2.4	31.5	25	65	-
[14]	2.4	21	33	180	0.9 × 0.6
This Work	1.85	29.1	> 31 (Max. PAE = 36 %)	130	1.0 × 1.7

the measured efficiency improvement was nearly 10%. Thus, the effect of the inter-stage capacitor on the overall efficiency was successfully verified.

Figure 12 shows the measured frequency responses for the two amplifiers. As expected, the efficiency of the proposed amplifier is always higher than that of the general amplifier in all measured ranges. Table 1 shows the summary of the comparison for the various fully-integrated RF CMOS power amplifiers.

7. CONCLUSION

In this work, we analyzed the effect of an inter-stage capacitor located between the power stage input and the driver stage output on the overall efficiency and on gate-drain reliability problems. The amplifier was designed using a class-D amplifier for the driver stage and a class-E amplifier for the power stage. The elimination of the inter-stage capacitor enhances the overall efficiency and moderates the gate-drain reliability problems. The analyzed effect of the inter-stage capacitor was verified successfully using the measured data.

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