Progress In Electromagnetics Research C, Vol. 18, 231–244, 2011

POWER SPLITTER ARCHITECTURES AND APPLICATIONS

M. Jalalifar

Department of Electrical and Computer Engineering
The University of Western Ontario
London, ON, Canada

M. J. Uddin

Department of Computer Science and Engineering
Asian University of Bangladesh
Dhaka, Bangladesh

Abstract—In order to use power splitter for communication and real world applications (e.g., telephony performances, antenna designs, wireless communications, digital communications, optical communications, CATV transmission systems, airborne systems), studying the nature and characteristics of the splitter is important. The purpose of this paper is to review and discuss various techniques aimed to develop the power splitters component and remove its interference. This paper further focuses on the review of future implementation techniques and performance comparison along with their applications. Some of the applications are illustrated at the end of the paper, and recommendation for further study is also outlined. This review serves as a comparative studies and reference beneficial for power splitter researchers and for future implementation of the technology. This review paper opens a corridor for researchers to perform future comparative studies between different architectures and models as a reference point for developing more powerful, flexible and efficient applications.

Received 10 October 2010, Accepted 2 December 2010, Scheduled 20 December 2010
Corresponding author: Majid Jalalifar (mjalalif@uwo.ca).

1. INTRODUCTION

In communication system, power splitter splits the power from one port to two or more ports in load circuits by a certain percentage. The power splitters generally employ quarterwave transmission line at the design of center frequency. It has unrealistic dimensions and low microwave bands where the wavelength is large [1]. Power splitter has a number of common components such as capacitors, inductors and resistors. There are various types of power splitters such as transformer type Wilkinson splitter, lumped element quadrature Wilkinson power splitter, hybrid splitter, phase splitter, and mixed lumped distributed element power splitter. Power splitters are designed to fit some standard frequency ranges such as low frequency (120–135 kHz), high frequency (10–15 MHz), ultra high frequency (UHF) (850–950 MHz), and microwave frequency (2.45 GHz) [2]. Nowadays, scientists are making power splitter using various processes and technologies to achieve low losses, low costs and to minimize the area. Typical process technologies are CMOS, BiCMOS, GaAs, FET, MESFET, printed circuit board (PCB), and Silk Screen. The key specifications of power splitter circuit design is to achieve low return loss, low insertion loss, high isolation loss, phase difference, gain, port matching, wide bandwidth, and compact size. At present time, power splitters are being used in a wide range of communication applications such as telephony performances, antenna designs, wireless communications, digital communications, optical communications, CATV transmission systems, airborne systems.

This review firstly gives a brief explanation about splitter and a short historical background of the entire systems. This is followed by highlighting the architectural infrastructure of power splitter. Furthermore, a brief explanation of theoretical analysis is reviewed. Moreover, power splitters circuit design perspective based on the frequency range and the different methods have been explained. The effects of power splitter performance and analysis have also been reviewed. Finally, power splitters have been used in different application ongoing researches.

2. A BRIEF HISTORY

It is very important to reduce the physical layout of power splitter. Typically to fabricate a 1 GHz power splitter, the quarter wave sections are laid out in microstrip on a soft substrate such as Duroid which would measure to be a couple of inches long. A brief history of the power splitter since it was invented in 1960 is described as follows.

In 1965, Parad and Moynihan showed Split Tee power divider which was unequal split [3]. They added Wilkinson circuit into their circuit as an input transformer. In 1968, Cohn presented an excellent design for multistage Wilkinson splitter. It showed broadband three port transverse electromagnetic (TEM) mode hybrids method. Cohn also presented a mathematical model of Wilkinson's power splitter using the even and odd mode analysis [4]. From the even and odd mode schematics, the reflection coefficients can be calculated from the impedance looking in (Z_{in}) using the transformer Equation (1):

$$Z_{\text{in}} = \frac{Z_L + JZ_C \tan(\beta l)}{Z_C + JZ_L \tan(\beta l)} \tag{1}$$

In 1975, Gysel designed a new N-way power splitter which was suitable for high power application [5]. It provides in-phase outputs which is configured most commonly as a two-port but can serve as an N-way splitter as well. The Webb's splitter technique was introduced in 1981 [6]. The proposed circuit used quarter wave technique where impedance was replaced with two transmission lines in series. In 1990, Ito presented distributed and lossy match active power splitter which was used in bridged T low pass filter networks [7]. Monolithic microwave integrated circuit (MMIC) active power splitter circuit was first designed by Kamitsuna and Ogawa, in 1993 [8]. The miniature ultra wideband MMIC active power splitters has arbitrary phase relationships, which are based on the FET's inherent phase inversion properties together with phase adjustment circuits. In 2003, Nagi presented a miniature lumped element 180° Wilkinson splitter [9]. It uses a conventional Wilkinson splitter, a negative and positive phase shifter. Two years later (2005), Esper-Chain et al. designed an asymmetrical power splitter based on high speed digital systems [10]. It enables inter-board connections without requiring a central switch fabric. However, the main drawback of the proposed multidrop serial link is the signal integrity degradation that imposes significant data rate limitations. To overcome this problem, in 2006, Mao and Chueh introduced composite right/left handed coplanar waveguide power splitter [11]. In 2007, Lee and Lai, presented low power and low cost CMOS active differential power splitter. This architecture was implemented using the TSMC 0.18 µm CMOS process [12]. It is easily integrated and suitable for system-on-a-chip (SoC) applications. In 2008, Wang et al. presented a new broadband miniature RF power splitter [13]. The design is based on a transformer-type Wilkinson power splitter. Figure 1 summarizes a background of splitter, which is divided into two categories as Wilkinson PS and other methods.

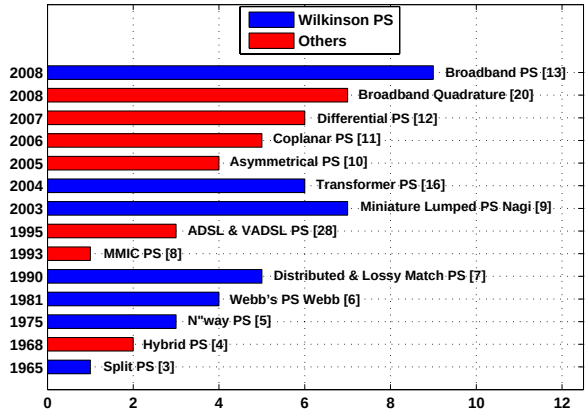

Figure 1. A brief background of power splitter.

3. EFFECTS OF POWER SPLITTER PERFORMANCE AND ANALYSIS

The main concern of power splitter circuit analysis is to achieve low return loss, low insertion loss, high isolation loss, phase difference, gain, port matching, good amplitude, wide bandwidth, and compact size. The review of different circuit outcomes and a comparison table is presented in this section.

According to Nagi in 2003, splitter circuit uses a negative and a positive phase shifter. The evaluated insertion loss is less than 1.1 dB [9]. The difference between output ports is simulated to be less than 0.35 dB. The entire system operates with 1.75 GHz bandwidth. The simulated and measured phase difference is within the expected range of $\pm 10^{\circ}$. In 2003, Ponchak et al. presented CMOS grade Si with a polyimide interface layer and embedded passives which yield significantly lower insertion loss [14]. The proposed design has very low insertion loss of only 0.57 dB, the return loss of 15 dB, and the isolation between Ports 2 and 3 of 20 dB. The design was modeled using electromagnetic (EM) software SONNET. In 2004, Campbell et al. presented 3 dB in phase splitter used in many RF and microwave systems [15]. The measured analysis and design use PSPICE and Hewlett Packard (HP) 8510 network analyzer. The circuit provides moderate insertion loss between 1.1 and 1.5 dB across the design bandwidth. Isolation and impedance match on all ports are more than 20 dB. The absolute phase difference between the two output ports is 0.4°. The 3 dB phase splitter circuit is operated across the 1.5 to 2.5 GHz range. In 2004, Kim et al. presented a transformer-type

lumped equivalent circuit using even and odd mode analysis [16]. It is operated in a bandwidth from 5 MHz to 1500 MHz frequency regions. The return loss and isolation value is lower than 15 dB. In 2007, Lee and Lai presented CMOS active differential power splitter [12]. This architecture not only offers high transfer power gain, but also adopts the tuning current source to overcome the power imbalance caused by process variation. The proposed design is operated in the frequency range from 3.5 GHz to 6 GHz. The designed circuit phase error is less than 7°, and the power imbalance is less than 1.4 dB. Moreover, the transfer power gain is 9.66 dB, return loss 5 dB, noise figure 4.35 dB, power consumption 15 mW and 1-V supply voltage respectively.

This architecture is different from the passive phase power splitter (PPS) architecture. The advantages are no conversion loss and a small chip area with 0.8 mm × 0.7 mm. The architecture is implemented by the TSMC 0.18 µm CMOS process. The splitter has low cost and possesses the characteristics of low voltage and low power. It is easy to integrate and suitable for system-on-a-chip applications. In 2008, Chen et al. presented a wideband mixed lumped distributed element 90° and 180° power splitter [17]. The 180° and 90° power splitters are based on mixed lumped-distributed-element three port Wilkinson power splitter with phase shifters at the outputs. It shows an amplitude balance

Table 1. Summary of major results.

Reference	Process	RF Frequency (GHz)	Insertion loss (dB)	Return loss (dB)	Isolation (dB)	Phase imbalance (Degree)
[9]	Thin Film	5.5	< 1.1	-	> 18	± 10
[14]	CMOS	12.5	0.57	26	20	120
[15]	GaAs	2	3	20	22	0.4
[16]	-	5–1500 (MHz)	6	< 15	< 15	-
[19]	-	8.2–12.4	0.7	15	-	180
[20]	-	14.5	-	18	-	-
[12]	CMOS	3.5–6	-	< 5	15	7
[21]	PCB	1.1–3.5	-	10	10	90
[17]	BiCMOS	70–80	-	12	-	90
[22]	Silk Screen	500 MHz–2 GHz	0.4	3	-	-
[23]	MESFET	0.5–20	-	-	-	35
[8]	FET	7.2–21.6	7	15	17	20
[24]	BiCMOS	1.5–1.8	-	-	40 and 50	150
[25]	BiCMOS	0.2–22	-	-	-	4

which is better than 0.05 dB and 0.21 dB, respectively. It is operated at 77 GHz. The return losses for both power splitters are better than 12 dB from 70 GHz to 80 GHz. The effective areas of the 180° and 90° splitters are $240 \times 440\,\mu m^2$ and $220 \times 400\,\mu m^2$, respectively. A summary of power splitter result is given in Table 1.

4. POWER SPLITTER CIRCUIT DESIGN PERSPECTIVE

In 1993, Kamitsuna and Ogawa, developed a circuit to achieve wideband phase splitting performance (other than 180°) with additional phase adjustment circuits [8]. The wideband active power splitter block diagram is shown in Figure 2. The proposed circuit uses common drain FET configuration because of its high input and low output impedance characteristics. Therefore, it allows us to rotate the phase significantly, as well as provides active matching. The differential phase splitter has used RF building block for ISM band (5.1–5.9 GHz) designed by Do et al. in 2003 [18].

The design goal is to achieve 180° phase difference and gain imbalance. The proposed design is achieved using Cadence Spectre RF Simulator and 0.18 μm CMOS process Design Kit (PDK). A conventional phase splitter is shown in Figure 3.

In 2004, Campbell et al. presented an integrated low pass broadband passive in-phase splitter [15]. The circuit is implemented on a standard GaAs process with three thick metal layers, high Q capacitors, high Q inductors, resistors and tightly coupled transformers. In microwave frequencies, bond wire parasitics can be absorbed into network reactance. An additional reactive element also

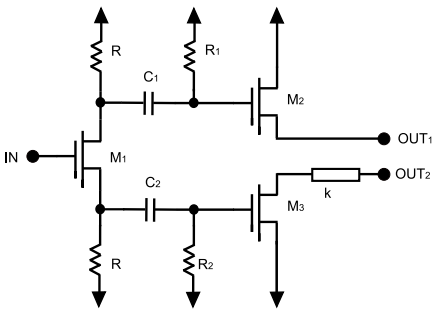

Figure 2. Circuit diagram of the wideband active splitter [8].

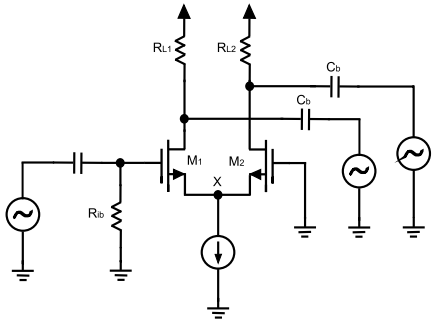

Figure 3. A conventional phase splitter [18].

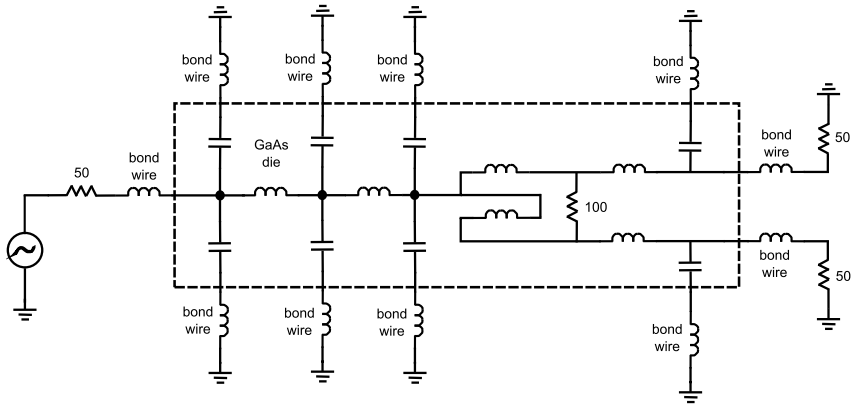

Figure 4. Schematic of the power splitter [15].

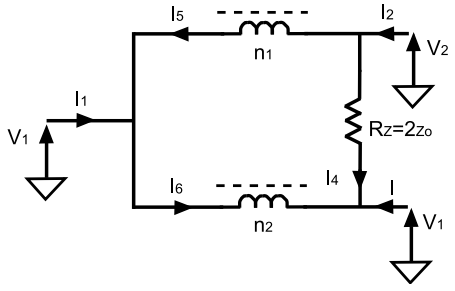

Figure 5. Equivalent circuit employing transformers [16].

can be added to the output ports for designing in a practical circuit implementation. A complete block diagram of splitter is shown in Figure 4.

The proposed circuit uses coupled transmission line transformer which offers very low loss to odd mode currents, while even-mode currents observe a large series inductive reactance. Based on coupled transmission idea, Kim et al. in 2004 presented transformer type Wilkinson power splitter with a compensating circuit [16]. It analyzes the frequency characteristics using even and odd mode method. Figure 5 shows the equivalent circuit employing transformer Wilkinson power splitter. The design of lumped quadrature power splitter (LQPS) based on unit cells of right handed (RH) and left handed (LH) synthetic transmission lines (TLs) were presented by Kuylenstierna et al. in 2005 [26].

The designed circuit shows how different out-of-phase power

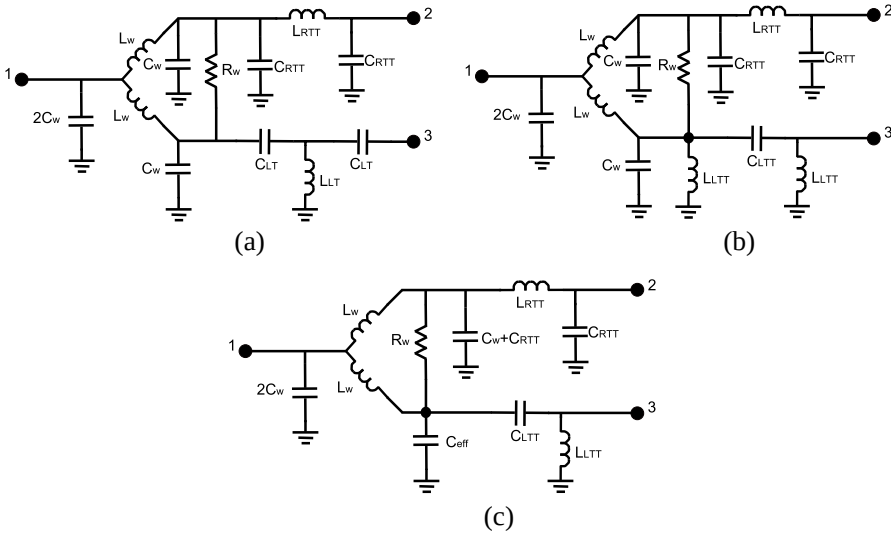

Figure 6. Three different LQPS. (a) $W_{R\pi\pi}R_{\pi}L_{T}$. (b) $W_{R\pi\pi}R_{\pi}L_{\pi}$. (c) Reduced $W_{R\pi\pi}R_{\pi}L_{T}$ [26].

splitters may be synthesized with right-handed (RH) and left-handed (LH) TLs. For derivation of analytical expressions, the RH/LH TLs are treated as symmetric unit cells (π or T networks). Figure 6 shows three different LQPS for their compactness, and electric $W_{R\pi\pi}R_{\pi}L_{T}$ LQPS has the same topology as the 180° out-of-phase power splitter. Figure 6(a) shows the $W_{R\pi\pi}R_{\pi}L_{T}$ LQPS infrastructure design. However, it is considered as a quadrature (90°) power splitter since the amplitude and phase errors are smaller over a larger bandwidth. The $W_{R\pi\pi}R_{\pi}L_{\pi}$ LQPS is shown in Figure 6(b). It includes one extra inductor, compared to the $W_{R\pi\pi}R_{\pi}L_{T}$ in Figure 6(a), but for properly chosen component values $L_{L\pi}$ in parallel with CW that can be replaced with an effective capacitor C_{eff}. Figure 6(c) is shown in $W_{R\pi\pi}R_{\pi}L_{T}$ LQPS.

In 2007, Yhland and Stenarson presented the uncertainty calculation together with a technique to assess the residual error, when calibrating the effective source match of power splitters [27]. This technique was the most convenient way of measuring the effective source match. The technique uses an airline as impedance reference which is similar to the ripple technique. It is used in evaluating the residual errors in vector network analyzers. The proposed circuit directly assesses the residual error and measurement uncertainty of γ_{eff}. γ_{eff} is expressed as a function of the S-parameters of the splitter

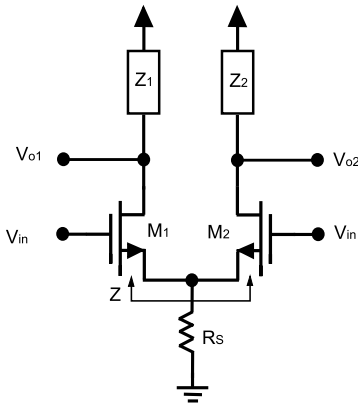

Figure 7. Simple PPS adopting differential amplifier topology [12].

as shown:

$$\gamma_{eff} = S_{22} + \frac{S_{21}S_{32}}{S_{31}} \tag{2}$$

The splitter uses a passive component that is operated in the Marchand-type or multiport couplers. For lower frequency applications, the coupler size increases rapidly, and it is very difficult to integrate. To overcome this problem, in 2007, Lee and Lai presented a differential amplifier architecture for designing power splitter [12]. Phase and power splitter (PPS) adopting differential amplifier topology is shown in Figure 7. Here, the phase difference can be adjusted by the RS impedance, sizes of transistors M_1 and M_2 and the load impedances Z_1 and Z_2. They replace R_S by a current tuner M_3 to restore the effect of the process variation.

5. APPLICATION OF POWER SPLITTERS

Recent communication equipment designs of power splitters have been rapidly growing. In this sense, researchers have focused on the development of low cost, high speed, low loss, and high reliability splitters. They are designing a number of methods, and it is used in many applications such as telephony performances, antenna designs, wireless communications, digital communications, optical communications, CATV transmission systems, and airborne systems. This section has been reviewed based on these applications.

By using asymmetric digital subscriber line (ADSL) technology and very high speed versions (VADSL) technology, power splitter can be utilized in the telephony transmission system. This

technology offers the opportunity to provide broadband service instantly without the need to wait for deployment of fiber in the access network. The proposed technology is vital if this interest is to be maintained. It also has the ability to support secure telephony simultaneously while delivering the broadband service [28]. At the Electromagnetic Institute, Technical University Lyngby, Denmark, electronics research group uses multimode interference power splitter for optical communications. Some of the important performance characteristics of such splitters have low losses and reflection, compatibility with optical single mode fibers, uniform distribution of the output power on the N waveguides and a low price. The proposed methods lead to process-tolerant design because the sharp edges near the branching points are avoided. This structure is inherent in the silica-on-silicon technology to produce in fiber-compatible integrated optical devices [29]. Mao and Chueh have been used composite right/left handed (CRLH) coplanar waveguide (CPW) power splitter for antenna applications [11]. The proposed structure shows not only superior phase and magnitude performance but also a 37% size reduction. Moreover, applications involving the wideband coplanar waveguide-to-coplanar stripline (CPW-to-CPS) transition and the tapered loop antenna are presented to stress the practicality of the 180 CRLH CPW power splitter. Nowadays, digital communication equipment designs have shown a rapidly growing need for higher bandwidth interconnection between printed circuit board (PCB) modules. Power splitters with good matching trace impedance are being used for high speed digital systems [10]. Later on, researchers focuse on system-on-a-chip for wireless communication application. They have invented phase and power splitter using the TSMC 0.18 μm CMOS process technology. Wireless communication techniques are employed not only in portable devices, but also in many new applications such as biochips, identifications, and intelligent electric appliances. These applications are in low power which is an increasingly important design issue [12]. Power splitter also can be used in CATV transmission systems [16]. In order to obtain the best RF performance, the power splitter has used an optimal RF design method which is followed by a transformer-type lumped equivalent circuit and an even/odd mode analysis. It is optimally designed using a newly proposed design method that employs transformer-type lumped equivalent circuit.

6. CONCLUSION

The review provides various design methodologies to achieve low return loss, low insertion loss, high isolation loss, phase difference, gain, port matching, good amplitude, wide bandwidth, and compact size for power splitters. The review has shown a high speed digital systems asymmetrical power splitters where inter-board connections can be used without requiring central switch fabric. We see that a major drawback of differential power splitter architecture not only offers high transfer power gain, but also adopts the tuning current source to overcome the power imbalance caused by process variation. The marchand-type or multiport couplers is not a suitable choice for low frequency applications, since their size increases rapidly. Moreover, it is difficult to integrate while it is on board. While reviewing the properties of differential power splitter, we find that the proposed architecture is different from the passive phase and power splitter. It has the advantages of no conversion loss and small chip size. It has been shown that the power splitters generally employ quarterwave transmission line sections at the design center frequency. Moreover, power divider or splitter can have unrealistic dimensions at frequencies in the RF and low microwave bands, where the wavelength is large. The study shows that multimode interference power splitter important performance characteristics are low losses and reflection, uniform distribution of the output power on the N waveguides and low price.

REFERENCES

1. Inc P-N Designs, "Wilkinson power splitters, Microwave 101," http://www.microwaves101.com/encyclopedia/Wilkinson splitters.cfm., Jun. 2008.
2. WJ Communications Inc., "A compact RFID reader platform for UHF and microwave applications," *Microwave Journal*, Vol. 47, No. 4, 1–4, Apr. 2004.
3. Parad, L. I. and R. L. Moynihan, "Split-tee power divider," *IEEE Transactions on Microwave Theory and Techniques*, Vol. 13, No. 1, 91–95, Jan. 1965.
4. Cohn, S. B., "A class of broadband three-port TEM-mode hybrids," *IEEE Transactions on Microwave Theory and Techniques*, Vol. 19, No. 2, 110–116, Feb. 1968.
5. Gysel, U. H., "A new N-way power divider/combiner suitable for high-power applications," *IEEE Transactions on Microwave Theory and Techniques*, Vol. 75, No. 1, 116–118, May 1975.

6. Webb, C. R., "Power divider/combiners: Small size, big specs," *Microwaves*, 67–74, Nov. 1981.
7. Ito, Y., "Distributed and lossy match active power splitters using bridgedCT low-pass filter networks," *IEEE MTT-S International on Microwave Symposium Digest*, Vol. 3, 1089–1092, May 1990.
8. Kamitsuna, H. and H. Ogawa, "Ultra-wideband MMIC active power splitters with arbitrary phase relationships," *IEEE Transactions on Microwave Theory and Techniques*, Vol. 41, No. 9, 1519–1523, Sep. 1993.
9. Nagi, H. S., "Miniature lumped element 180° a Wilkinson divider," *IEEE MTT-S International Microwave Symposium Digest*, Vol. 1, 55–58, Jun. 2003.
10. Esper-Chain, R., F. Tobajas, O. Tubio, R. Arteaga, V. de Armas, and R. Sarmiento, "A gigabit multidrop serial backplane for high-speed digital systems based on asymmetrical power splitter," *IEEE Transaction on Circuits and Systems II: Express Briefs*, Vol. 52, No. 1, 5–9, Jan. 2005.
11. Mao, S. G. and Y. Z. Chueh, "Broadband composite right/left-handed coplanar waveguide power splitters with arbitrary phase responses and balun and antenna applications," *IEEE Transactions on Antennas and Propagation*, Vol. 54, No. 1, 243–250, Jan. 2006.
12. Lee, S. Y. and C. C. Lai, "A 1-V wideband low-power CMOS active differential power splitter for wireless communication," *IEEE Transactions on Microwave Theory and Techniques*, Vol. 55, No. 8, 1593–1600, Aug. 2007.
13. Wang, Y. X., H. Q. Hu, and J. Xu, "A new broadband miniature RF power splitter," *IEEE MTT-S International Microwave Workshop Series on Art of Miniaturizing RF and Microwave Passive Components*, Vol. 1, 180–182, Dec. 2008.
14. Ponchak, G. E., A. Bacon, and J. Papapolymerou, "Monolithic wilkinson power divider on CMOS grade silicon with a polyimide interface layer for antenna distribution networks," *IEEE Antennas and Wireless Propagation Letters*, Vol. 2, 167–169, Aug. 2003.
15. Campbell, R., C. Microtech, and T. White, "Monolithic GaAs passive lowpass 3 dB in-phase splitter/combiner," *High Frequency Design GaAs Splitter/Combiner*, Jul. 2004.
16. Kim, D. I., S. W. Jung, and Y. Yun, "A high performance transformer-type Wilkinson power splitter with compensating circuit for CATV transmission system and its optimal design method," *IEEE Transactions on Consumer Electronics*, Vol. 50, No. 3, 934–940, Aug. 2004.

17. Chen, A. Y. K., H. B. Liang, Y. Baeyens, Y. K. Chen, J. Lin, and Y. S. Lin, "Wideband mixed lumped-distributed-element 90° and 180° power splitters on silicon substrate for millimeterwave applications," *IEEE Radio Frequency Integrated Circuits Symposium*, 449–452, Jun. 2008.
18. Do, M. A., W. M. Lim, J. G. Ma, and K. S. Yeo, "Design of a phase splitter for 3rd ISM band," *IEEE Conference on Electron Devices and Solid-States Circuits*, 237–240, Dec. 2003.
19. Lou, Y., Q. Xue, and C. H. Chan, "A broadband waveguide-tomicrostrip transition/power splitter using finline arrays," *IEEE Microwave and Wireless Components Letters*, Vol. 17, No. 4, 31312, Apr. 2007.
20. Chu, Q.-X. and R. Dong, "A novel multi-channel spatial power splitter," *International Conference on Microwave and Millimeter Wave Technology*, 1–3, Apr. 2007.
21. Tseng, C.-H. and C.-L. Chang, "A broadband quadrature power splitter using metamaterial transmission line," *IEEE Microwave Wireless Components Letters*, Vol. 18, No. 1, 25–27, Jan. 2008.
22. De Melo, M T., B. G. M. de Oliveira, L. L. D. Cabral, and E. J. P. Santos, "Coplanar power splitter analysis for the miniaturization of instantaneous frequency measurement subsystems," *International Conference on Microwave and Telecommunication Technology*, 449–451, Sep. 2001.
23. Baree, A. H. and I. D. Robertson, "Monolithic MESFET distributed baluns based on the distributed amplifier gateline termination technique," *IEEE Transactions on Microwave Theory and Techniques*, Vol. 45, No. 2, 188–195, Feb. 1997.
24. Lin, J., C. Zelley, O. Boric-Lubecke, P. Gould, and R. Yan, "A silicon MMIC active balun/buffer amplifier with high linearity and low residual phase noise," *IEEE Transactions on Microwave Theory and Techniques Digest*, 1289–1292, 2000.
25. Viallon, C., D. Venturin, J. Graffeuil, and T. Parra, "Design of an original k-band active balun with improved broadband balanced behavior," *IEEE Microwave and Wireless Components Letters*, Vol. 5, No. 4, 280–282, Apr. 2005.
26. Kuylenstierna, D., S. E. Gunnarsson, and H. Zirath, "Lumpedelement quadrature power splitters using mixed right/left-handed transmission lines," *IEEE Transactions on Microwave Theory and Techniques*, Vol. 53, No. 8, 2616–2621, Aug. 2005.
27. Yhland, K. and J. Stenarson, "Measurement uncertainty in power splitter effective source match," *IEEE Transactions on Instrumentation and Measurement*, Vol. 56, No. 2, 669–672,

Apr. 2007.

28. Cook, J. and P. Sheppard, "ADSL and VADSL splitter design and telephony performance," *IEEE Journal on Selected Areas in Communications*, Vol. 13, No. 9, 1634–1641, Dec. 1995.
29. Rasmussen, T., J. K. Rasmussen, and J. H. Povlsen, "Design and performance evaluation of 1-by-64 multimode interference power splitter for optical communications," *Journal of Lightwave Technology*, Vol. 13, No. 10, 2069–2074, Oct. 1995.