

Compact Active Duplexer Based on CSRR and Interdigital Loaded Microstrip Coupled Lines for LTE Application

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Abstract—In this paper, a four-port compact active duplexer based on a complimentary split ring resonator (CSRR) and interdigital loaded microstrip coupled lines (CSRR-IL MCL) is presented. Interdigital capacitor is used on the top layer of the proposed structure and CSRR transmission lines are used on the bottom layer of the coupled lines in order to increase the coupling of the proposed circuit and create triple band resonances, respectively. The proposed active duplexer has one input port and three output ports operating in three distinct operation frequencies which are 1.4 GHz, 1.8 GHz, and 3.2 GHz. The active duplexer is designed to target LTE applications which are prevalent among the new technologies and devices. The input signal is split in terms of frequency into the three designed frequencies and is amplified by 13 dB gain of the amplifiers placed at the output ports. The fractional bandwidths of the proposed structure at 1.4 GHz, 1.8 GHz, and 3.2 GHz are 5.2%, 2.8%, and 9.4%, respectively. It is worth mentioning that the size of the proposed active duplexer is $0.29\lambda_0 \times 0.38\lambda_0$. The design guide of the proposed structure is presented, and it will be shown that the simulation as well as the measurement results of the proposed active duplexer have an acceptable agreement with each other. It should be noted that the VSWR of the proposed structure is less than 1.5 which means that the active duplexer has low return loss, and it is the plus point of it.

1. INTRODUCTION

The duplexer is a key component in wireless communication. By using this component, receiver and transmitter modules can share one antenna, so more compact size and lower cost can be achieved by using duplexer in the transceivers [1]. In the conventional duplexers, passive filters are used which can create insertion loss in the path of the signal [2, 3]. There are some other ways to implement duplexer in the literature including surface acoustic wave (SAW) [4, 5] and ceramic cavities. Although the previous works on duplexer were good progress in the field of designing duplexers, they suffer from some drawbacks such as high cost, being bulky and non-integrable with other components in the transceiver.

After the introduction of metamaterial by Pendry et al. [6], a window of opportunities has been opened to electrical engineers to design novel devices and components. To implement metamaterials with microstrip transmission lines, composite right/left-handed (CRLH) transmission lines are proposed [7, 8]. There are different types of CRLH transmission lines that can be realized including interdigital and complementary split-ring resonator (CSRR) [7, 9]. CRLH transmission lines can be potentially employed in the wide variety of passive components such as filter [10–12], power divider [13–15], coupler [16–18], antenna [19–21], and triplexer [22, 23]. Likewise, CRLH transmission lines can be utilized in active components, namely power amplifiers [24–26] and distributed amplifiers [27–29].

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In this paper, a four-port active duplexer, which has one input port and three output ports, based on CSRR and interdigital-loaded microstrip coupled lines (CSRR-IL MCL) is presented. The schematic of the general operation of the proposed structure is shown in Fig. 1. As can be seen from Fig. 1, if a spectrum containing three desired frequencies, i.e., f_1 , f_2 , and f_3 , inputs the proposed structure, these frequencies multiplex into three output ports, each of which works at a given frequency. It should be mentioned that the amplitude of the input signal is amplified by the proposed structure, hence the proposed structure is an active duplexer. The output ports of the active duplexer can be connected to either receivers or transmitters operated at the frequencies of the ports.

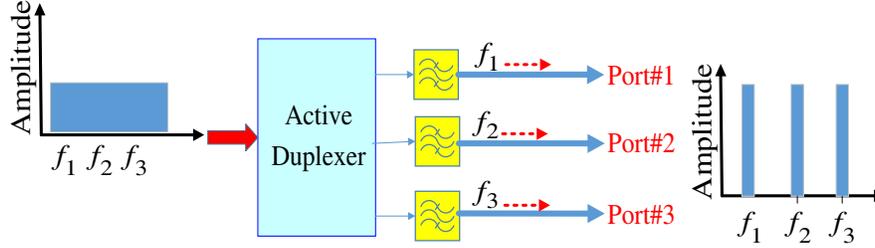


Figure 1. Operation of the active duplexer.

The paper is organized as follows. In Section 2, the design procedure of the proposed structure is presented. Next, the simulation and measurement results of the active duplexer are presented Section 3. Finally, the major points of the paper are recapitulated in Section 4 as the conclusion section of the paper.

2. DESIGN OF ACTIVE DUPLEXER

The proposed active duplexer consists of two parts, which are passive and active ones. The schematic of the proposed active duplexer is depicted in Fig. 2. When it comes to the passive part of the proposed structure, CSRR and interdigital-loaded microstrip coupled lines (CSRR-IL MCLs) are used. In CSRR-IL MCLs, two microstrip coupled lines are loaded with three unit cells of CSRR on the bottom layer and an interdigital capacitor on the top layer.

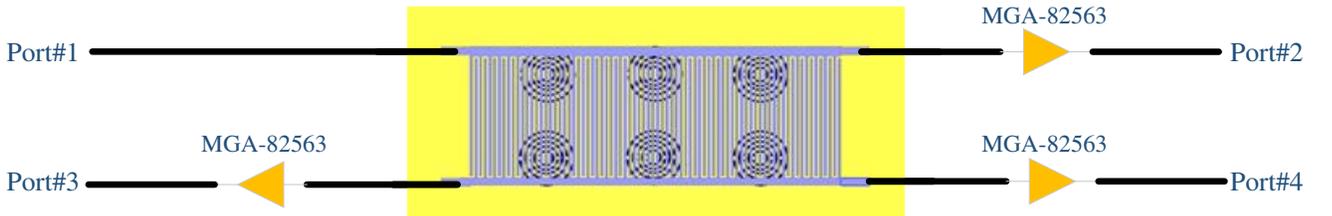


Figure 2. Proposed active duplexer.

The equivalent circuit model of the passive part of the proposed active duplexer is demonstrated in Fig. 3. The circuit model of CSRR transmission lines in the lower and upper rows of CSRR-IL MCL along with the circuit model of the interdigital capacitor of CSRR-IL MCL are indicated in Fig. 3. It is worth mentioning that the loss of the lines is considered in the proposed circuit model. The parameters of the circuit model should be extracted so as to make us capable of designing the passive part of CSRR-IL MCL. The values for the impedance and admittances of the circuit are presented in Eqs. (1)–(3).

$$Z = R + j\omega L \quad (1)$$

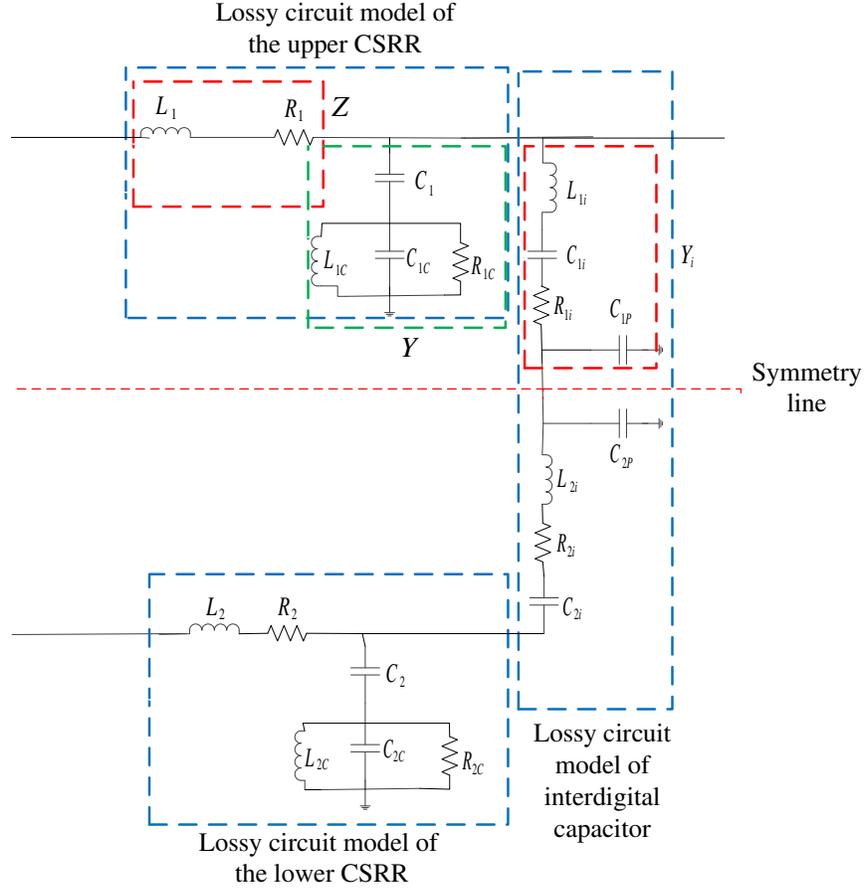


Figure 3. Circuit model of the passive part.

$$Y' = \frac{j\omega CR_c - j\omega^3 L_c C_c R_c C - \omega^2 L_c C}{-\omega^2 L_c C_c R_c + R_c + j\omega L_c - \omega^2 L_c R_c C} \quad (2)$$

$$Y_i = \frac{j\omega C_i}{1 - \omega^2 L_i C_i + j\omega R_i C_i} \quad (3)$$

where Z is the series impedance related to the circuit model of the CSRR transmission line, Y' the admittance in the shunt branch of the circuit model of the CSRR transmission line, and Y_i the admittance of the interdigital transmission line.

For the analysis of the circuit, the even and odd mode analysis is utilized. In the even mode analysis, the symmetry line acts as an open circuit, and in the odd mode analysis the symmetry line acts as a virtual ground. Accordingly, the equations for the even and odd mode analysis of the proposed circuit are presented in Eqs. (4) and (5), respectively.

$$Y_e = Y' + Y_m, \quad Z_e = Z \quad (4)$$

$$Y_o = Y' + Y_i, \quad Z_o = Z \quad (5)$$

where Y_e , Z_e , Y_o , and Z_o are the admittance of the even mode analysis, the impedance of even mode analysis, the admittance of the odd mode analysis, and the impedance of odd mode analysis, respectively.

Likewise, Y_m and C'_i are equal to $Y_m = \frac{j\omega C'_i}{1 - \omega^2 L_i C'_i}$ and $C'_i = C_i + C_p$. According to [30], two general equations are always valid in coupled transmission lines which are presented in Eqs. (6) and (7).

$$\cosh \gamma l = 1 + ZY \quad (6)$$

$$Z_c^2 = Z_{ce} Z_{co} \quad (7)$$

where γ is the propagation constant, l the length of the transmission line, Z_c the characteristic impedance of the coupled line, and Z_{ce} and Z_{co} are the characteristic impedances in even and odd modes, respectively. It is obvious that by using Eqs. (1)–(5), the right-hand side of Eq. (6) can be attained. When it comes to the relations for Z_{ce} , Z_{co} , and Z_c , some straightforward analyses can be done, and their results are as follows.

$$Z_{ce} = \sqrt{\frac{Z_e}{Y_e}} = \sqrt{\frac{Z}{Y' + Y_m}} = \sqrt{\frac{R + j\omega L}{\frac{j\omega CR_c - j\omega^3 L_c C_c R_c C - \omega^2 L_c C}{-\omega^2 L_c C_c R_c + R_c + j\omega L_c - \omega^2 L_c R_c C} + \frac{j\omega C'_i}{1 - \omega^2 L_i C'_i}}} \quad (8)$$

$$Z_{co} = \sqrt{\frac{Z_o}{Y_o}} = \sqrt{\frac{Z}{Y' + Y_i}} = \sqrt{\frac{R + j\omega L}{\frac{j\omega CR_c - j\omega^3 L_c C_c R_c C - \omega^2 L_c C}{-\omega^2 L_c C_c R_c + R_c + j\omega L_c - \omega^2 L_c R_c C} + \frac{j\omega C_i}{1 - \omega^2 L_i C_i + j\omega R_i C_i}}} \quad (9)$$

$$Z_c = \sqrt{Z_{ce} Z_{co}} = \sqrt[4]{\frac{R + j\omega L}{\frac{j\omega CR_c - j\omega^3 L_c C_c R_c C - \omega^2 L_c C}{-\omega^2 L_c C_c R_c + R_c + j\omega L_c - \omega^2 L_c R_c C} + \frac{j\omega C'_i}{1 - \omega^2 L_i C'_i}}} \times \sqrt[4]{\frac{R + j\omega L}{\frac{j\omega CR_c - j\omega^3 L_c C_c R_c C - \omega^2 L_c C}{-\omega^2 L_c C_c R_c + R_c + j\omega L_c - \omega^2 L_c R_c C} + \frac{j\omega C_i}{1 - \omega^2 L_i C_i + j\omega R_i C_i}}} \quad (10)$$

$$\gamma_e = \sqrt{R + j\omega L} \sqrt{\frac{j\omega CR_c - j\omega^3 L_c C_c R_c C - \omega^2 L_c C}{-\omega^2 L_c C_c R_c + R_c + j\omega L_c - \omega^2 L_c R_c C} + \frac{j\omega C'_i}{1 - \omega^2 L_i C'_i}} \quad (11)$$

$$\begin{aligned} \gamma_o &= \sqrt{Z} \sqrt{Y' + Y_i} \\ &= \sqrt{R + j\omega L} \sqrt{\frac{j\omega CR_c - j\omega^3 L_c C_c R_c C - \omega^2 L_c C}{-\omega^2 L_c C_c R_c + R_c + j\omega L_c - \omega^2 L_c R_c C} + \frac{j\omega C_i}{1 - \omega^2 L_i C_i + j\omega R_i C_i}} \end{aligned} \quad (12)$$

Afterward, some criteria should be imposed on the coupled lines in order to make us capable of designing the structure. These criteria can be achieved by considering the coupled lines in three ways, which are forward coupling, backward coupling, and the through direction. These three paths are always applicable to any types of coupled lines.

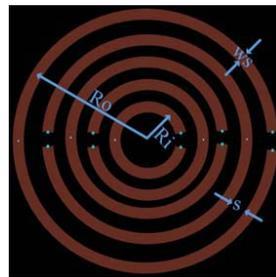
As regards the forward coupling, according to Fig. 2, the signal should go to port#4 when the input port is port#1. Hence, $|S_{41}|$ should be maximized in this case, which is $S_{41} = \frac{\sqrt{1-k^2}}{\sqrt{1-k^2} \cos \theta + j \sin \theta}$ according to [30], where $\theta = \gamma l$ and k is the coupling coefficient which is $k = \frac{Z_{ce} - Z_{co}}{Z_{ce} + Z_{co}}$. With respect to backward coupling, the signal should go from the input port, i.e., port#1, to port#3, so $|S_{31}|$ should be maximized. The equation for S_{31} in terms of coupling coefficient as well as propagation constant is $S_{31} = \frac{jk \sin \theta}{\sqrt{1-k^2} \cos \theta + j \sin \theta}$. Finally, the signal should go to port#2 in through direction, hence if we have $S_{21} = \sin\left(\left(\frac{\gamma_e - \gamma_o}{2}\right) l\right)$, $|S_{21}|$ should be maximized in this case.

After the determination of the criteria for different signal paths, by choosing the desired operating frequency for each port and $Z_c = 50$, the parameters in the circuit model will be achieved as in Table 1. It should be noted that the frequencies chosen for each port should be in LTE bands, because the proposed structure is designed to target LTE applications. According to these values for the lumped elements, the equivalent microstrip lines as well as CSRR transmission lines and interdigital capacitor are achieved. Because the losses of the transmission lines are negligible, they are not reported in Table 1.

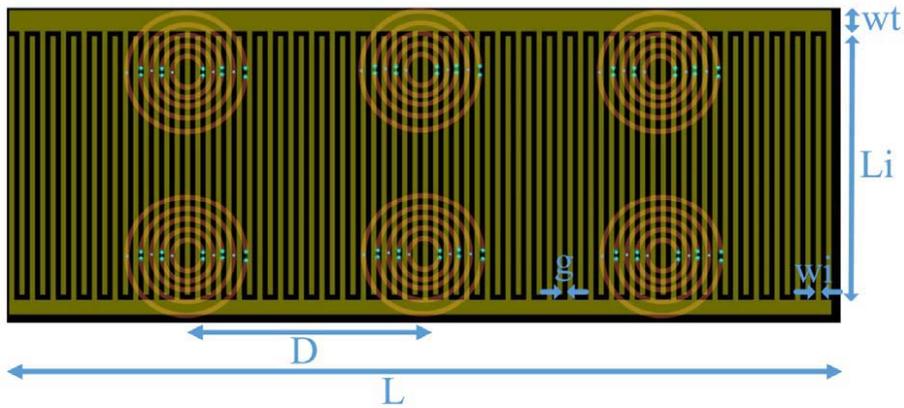
Having determined the passive part of the proposed active duplexer, the active part of the proposed active duplexer should be determined. For this purpose, an active component should be used such as a transistor. For the convenience of the design, the input impedance of the transistor and the output impedance of each port of the passive part are considered to be 50 ohms. In the next section, the simulation and measurement results according to the chosen transistor are to be presented.

Table 1. Lumped elements values in the circuit model.

Element	Value
L_1	9.8 nH
L_c	12.8 nH
L_i	10.8 nH
C_1	7.5 pF
C_c	6.4 pF
C_i	11.5 pF
C_p	7.3 pF



(a)



(b)

Figure 4. Dimensions of the proposed structure. (a) CSRR, and (b) passive part of the proposed active duplexer.

The unit cell of CSRR transmission line that is used to create active duplexer and the total passive part of the active duplexer are shown in Fig. 4. According to the lumped elements values presented in Table 1, the detailed dimensions of both CSRR transmission line unit cell and passive part of the active duplexer are specified as presented in Table 2.

3. RESULTS

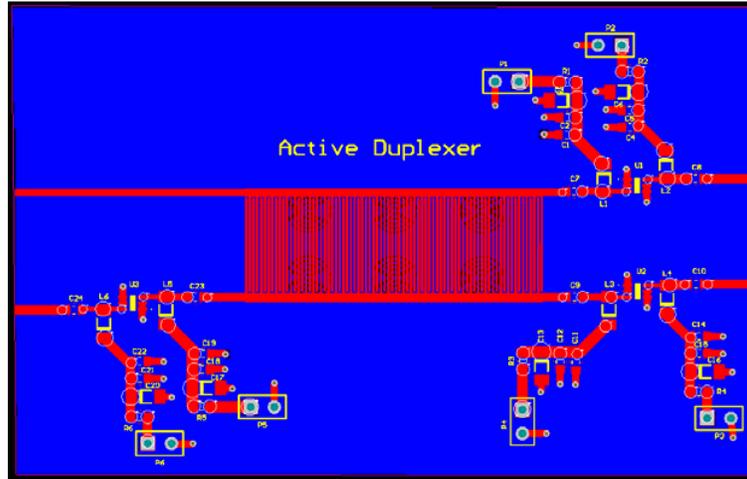
In this section, the results of the proposed active duplexer including simulation and measurement results are presented. At first, the desired frequencies in each output port are chosen as 1.4 GHz, 1.8 GHz, and 3.2 GHz. These frequencies are chosen for LTE applications. When it comes to the active part of the active duplexer, MGA-82563 which is an amplifier made by Avago Tech company is used. MGA-82563

Table 2. Detailed dimensions of the proposed active duplexer.

Dimension	Value
R_i	0.56 mm
R_o	2.4 mm
ws	0.2 mm
s	0.2 mm
wt	0.7 mm
L_i	10.2 mm
w_i	0.2 mm
g	0.2 mm
L	31.8 mm
D	9.2 mm

is a GaAs amplifier in which its operating frequency is from 0.1 GHz to 6 GHz. For the biasing of the transistor, an appropriate quiescent point should be considered in order to achieve the best results from the transistor, so $V_{GS} = 0$ V, $V_{DS} = 3$ V, and $I_{DS} = 80$ mA is considered as the quiescent point of the transistor.

The proposed active duplexer including passive and active part is implemented on an RO4003 substrate with $\epsilon_r = 3.38$, $\tan \delta = 0.0022$, and $h = 0.5$ mm, where ϵ_r , $\tan \delta$, and h are relative permittivity, loss tangent, and substrate height, respectively. For the simulation of the proposed active duplexer, advanced design system (ADS) software is utilized. Both momentum and schematic of ADS software are used in order to achieve accurate results. As regards the fabrication of the proposed structure, the layout of the active duplexer is prepared as Fig. 5.

**Figure 5.** Layout of the active duplexer.

As shown in Fig. 5, the layout consists of passive and active parts connected to each other. A T-bias circuit is chosen for the bias circuit of the active part as depicted in Fig. 6.

As shown in Fig. 6, two bias circuits which are similar to each other are used in the input and output ports of the amplifier, because sometimes it is needed to connect the Gate of the transistor to the different voltage sources in order to test the circuit. Moreover, three capacitors with different values are used in the bias circuit, because when we have an AC signal, the inductor is not short circuit in

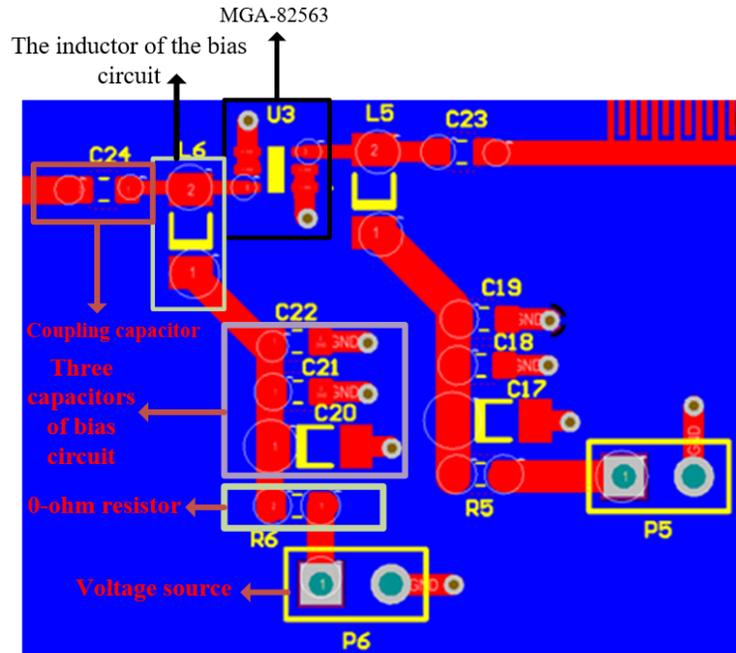


Figure 6. Amplifier with its bias circuit.

reality, and the AC part of the circuit should be isolated from the DC source by connecting the other terminal of the inductor to the ground by using these capacitors which act as short circuit in AC. The reason behind the different values of the capacitors is that the capacitors should be zero in different operating frequencies, and this can be achieved by using different values of the capacitance to have zero impedance in different operating frequencies.

The values of the lumped elements used in the bias circuit as well as the coupling capacitor are shown in Table 3. It is worth mentioning that the DC voltage is 3 volt.

Table 3. Lumped elements values of the bias circuit.

Element	Value
Coupling capacitor	5.6 pF
Three capacitors in the bias circuit	100 pF, 100 nF, 10 nF
Inductor in the bias circuit	22 nH

According to the aforementioned points, the proposed active duplexer is fabricated which is depicted in Fig. 7. It is notable that the size of the proposed active duplexer is $0.29\lambda_0 \times 0.38\lambda_0$.

After the fabrication of the proposed active duplexer, a vector network analyzer (VNA) should be used to do the measurement of the proposed structure and achieve its *S*-parameters. Therefore, the simulation and measurement results are shown in Fig. 8.

As can be seen from Fig. 8, each port operates at a given frequency which is different from the others. At 1.4 GHz, the input signal goes to port#4, and other ports are isolated from it. When it comes to 1.8 GHz, port#2 is the output port, and the others are isolated. When we use port#3 of the proposed active duplexer as the output port and other ports are isolated from it, we have backward coupling which can be achieved at 3.2 GHz operating frequency as shown in Fig. 8. It should be noted that all of the signals at the output ports are amplified and have approximately the same level. Hence, according to the presented measurement and simulation results, the proposed structure potentially serves as an active duplexer for LTE application. It is worth mentioning that the reason behind the

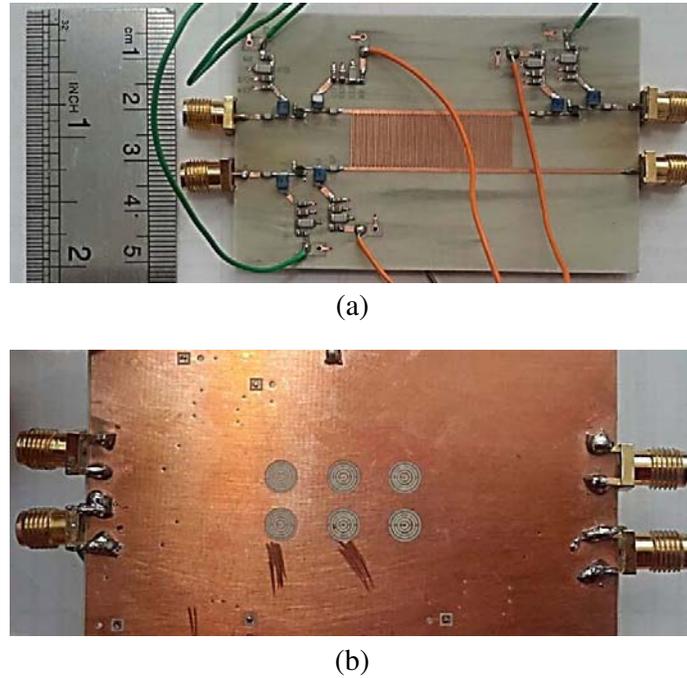


Figure 7. Fabricated active duplexer. (a) Top view, and (b) bottom view.

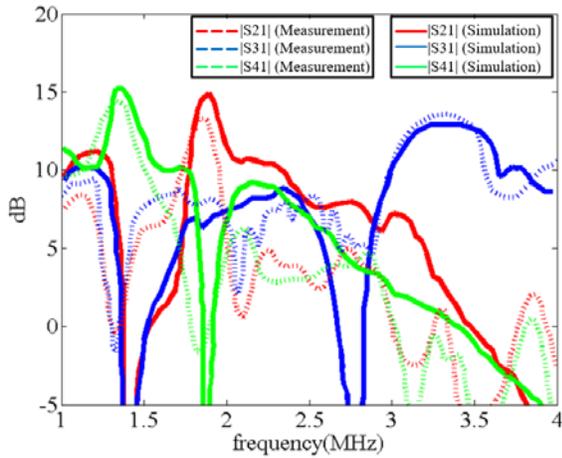


Figure 8. Simulation and measurement results of S -parameters.

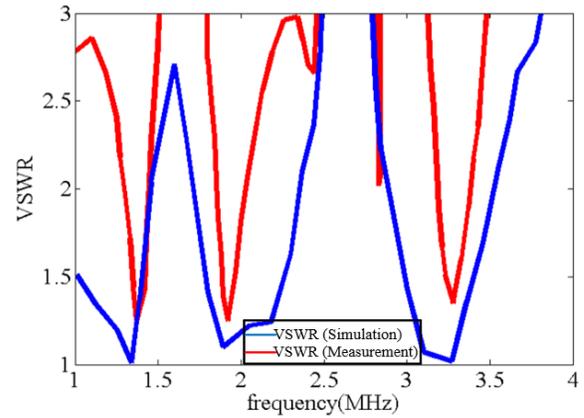


Figure 9. Simulation and measurement results of VSWR of the proposed active duplexer.

slight difference in the signal level at the output ports is the different insertion loss of each path which is not the same for various output paths.

Moreover, the voltage standing wave ratio (VSWR) can be presented in order to indicate the return loss of the proposed structure which is shown in Fig. 9. The minimum VSWR is 1 which means that return loss is zero, so the intention is to have VSWR close to 1 at operating frequencies.

The effects of the parameters including the radius of the CSRRs (R), the number of rings of the CSRRs (N), and the distance between the unit cells (D) on S -parameters are depicted in Fig. 10. The increment or decrement steps for changing R , N , and D with respect to the optimum values are 0.1 mm, 1, and 0.1 mm, respectively. As shown in Fig. 10, the optimum results are specified by solid lines, and the dotted lines are related to the effects of the mentioned parameters which are unwanted. It should

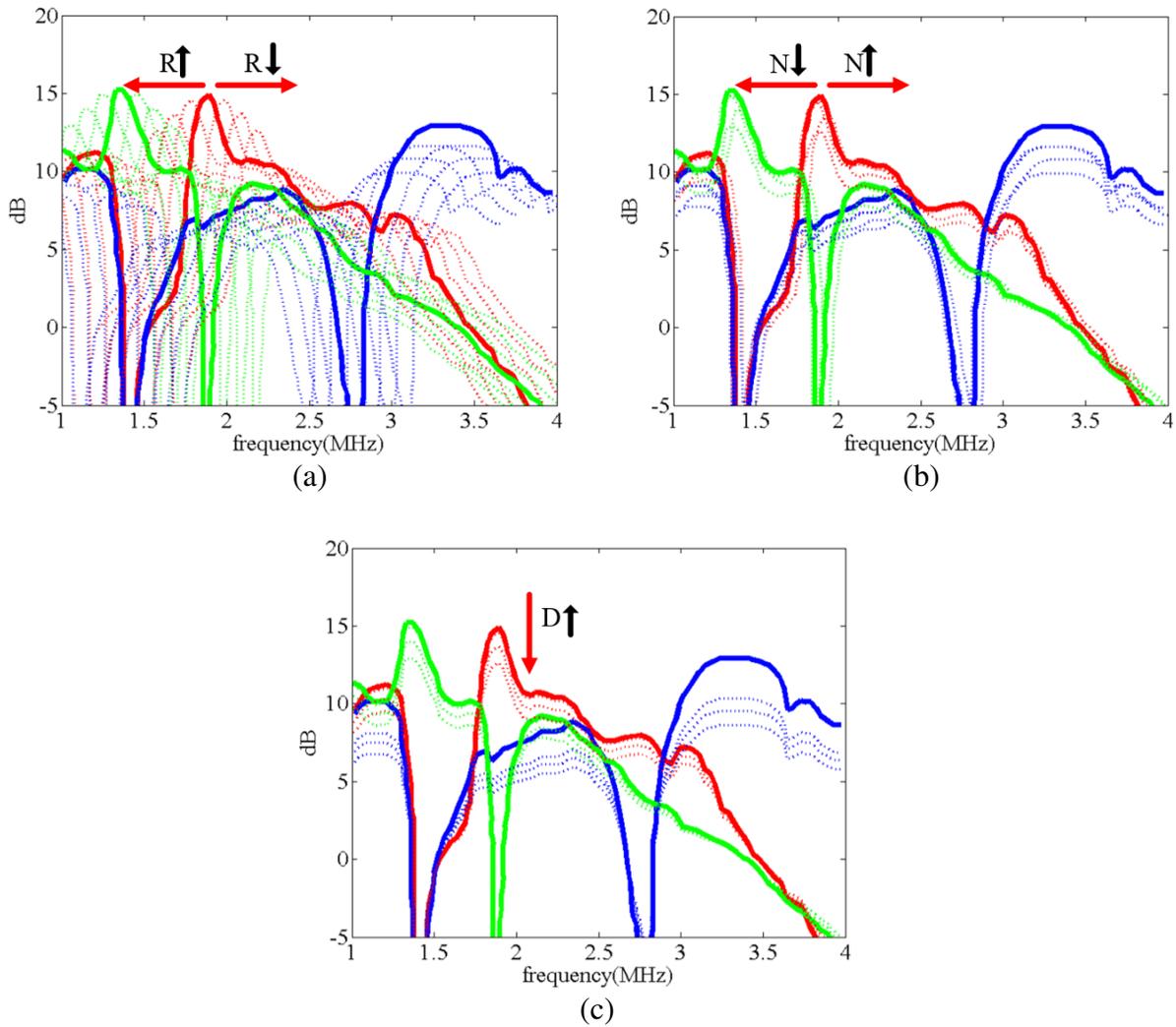


Figure 10. Effects of different parameters on the *S*-parameters results. (a) Radius of CSRRs, (b) number of rings of CSRRs, and (c) distance between the unit cells.

be noted that by changing *N* and *D*, the isolation of the proposed active duplexer will be decreased which is undesirable. When it comes to the radius of the CSRRs, i.e., *R*, the center frequency of the bands will be changed along with reducing the isolation in the bands.

According to the presented results, the table of comparison between the proposed active duplexer and its counterparts is presented in Table 4.

Table 4. Table of comparison between this work and other works.

References	Channels (GHz)	Technology	Duplexer/Diplexer type	Fractional Bandwidth (%)	Return Loss (dB)	Isolation (dB)	Size (mm ²)
[31]	1.6, 2.2	0.18 μm CMOS	Active	18.75, 17.25	20	40	0.013λ ₀ × 0.013λ ₀
[32]	1.9	N/A	Active/Passive	4.2	6	45	N/A
[33]	1.5, 2.6	SMT/PCB	Active	13.3, 36	20, > 10	25, 30	N/A
This Work	1.4, 1.8, 3.2	SMT/PCB	Active	5.2, 2.8, 9.4	25, 20, 20	25, 25, 20	0.29λ ₀ × 0.38λ ₀

4. CONCLUSION

In this paper, the design procedure and simulation and measurement results of a four-port active duplexer are presented. What sets this proposed active duplexer apart from the others is the fact that it enjoys a compact size, which is $0.29\lambda_0 \times 0.38\lambda_0$. The proposed active duplexer can be used in LTE applications according to the operating frequencies of the output ports of it. Furthermore, it is shown in the paper that measurement and simulation results have good agreement with each other which means that the design procedure and the formulas for the active duplexer are valid.

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