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# SILICON BASED VERTICAL MICRO-COAXIAL TRANSITION FOR HIGH FREQUENCY PACKAGING TECHNOLOGIES

**Justin Boone*, Subramanian Krishnan, and Shekhar Bhansali**

Department of Electrical and Computer Engineering, College of Engineering, Florida International University, Miami, FL 33174, USA

**Abstract**—A through wafer vertical micro-coaxial transition flushed in a silicon substrate has been designed, fabricated, and tested. The transition has been designed using radio frequency (RF) coaxial theory and consists of a 100 µm inner diameter and a 300 µm outer diameter, which corresponded to a 1 : 3 inner/outer diameter ratio. The transition's through silicon structure has been achieved using standard photolithography techniques and Bosch's process for deep reactive ion etching (DRIE). The coaxial vias of the transition have been successfully metalized with a diluted silver paste using a novel filling method. To measure the behavior of the transition at high frequencies, coplanar waveguide (CPW) lines matched at 50 ohms have been integrated on the front and backside of the device. Measurement results show that the transition demonstrate good results with a reflection coefficient better than −10 dB at high frequencies from 15 GHz-to-60 GHz. Results also indicate that the transition has good signal transmission with less than −1.8 dB insertion loss up to 65 GHz. By eliminating the need for rigorous bonding techniques, the transition is a low-cost and durable design that can produce high input/output ratios ideal for commercial products.

## 1. INTRODUCTION

In the RF module industry, transitions/interconnects are currently used for monolithic microwave integrated circuits (MMICs), multiple integrated circuit (IC) technologies, or 3-D integration of mm-wave passive devices [1–5]. More specifically, three-dimensional coaxial

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* Corresponding author: Justin Boone (jboon007@fiu.edu).

transitions have been highly useful by assisting in the development of compact multi-layer transmit/receiving systems. These transitions provide signal transmission through multi-layer mm-wave systems that require integrated circuits, RF sensors, and active and passive components to be integrated into a single package. Specifically, the best coaxial performance can be achieved by using a low permittivity and high resistivity dielectric [6]. This type of dielectric can also reduce the diameter ratio and transition size, which reduces capacitance issues that can surface through the inner dielectric as the frequency range increases. Although wire and flip-chip bonding has been successful approaches in the past [7], it suffers from many electrical drawbacks and thermo-compression issues [8]. Avoiding these design issues has been the driving force in the development of three-dimensional vertical coaxial transitions capable of integrating with high frequency packaging technologies.

Coaxial transitions are primarily determined by their inner and outer diameter ratios. Based on the dielectric being used and its resistivity, the proper diameter ratio must be selected in order to maximize performance. As indicated above, it is also important to consider the permittivity and loss tangent values of the chosen dielectric to avoid any reductions in signal propagation and overall transition size.

To the best of our knowledge, previous results in literature include quasi-coaxial approaches to develop high frequency transitions [9–11]. A microwave crossover system using a double microstrip CPW vertical interconnect was developed by Wang et al. [12], while [13] presents vertical coaxial transitions using C-shaped bump pads. In this work, we present the design of a vertical micro-coaxial transition within a 300 µm thick high-resistive silicon substrate. A silicon substrate was chosen because of its low-cost and easy integration abilities with commercial fabrication technologies. The transition demonstrated exceptional performance at millimeter wave frequencies while operating from dc-to-65 GHz, proving its ability to be used in high frequency packaging technologies.

## 2. MICRO-COAXIAL TRANSITION DESIGN

The layout of the proposed vertical micro-coaxial transition is shown in Figure 1. When using silicon as a dielectric, the inner/outer conductor ratio must be carefully determined to avoid frequency limitations and to achieve desired performance. These frequency limitations are due to the propagation of $TE_{nm}$ modes which are caused by the transitions circular waveguide structure. The first higher order mode to propagate

in the coax is the $TE_{11}$; where $n = 1$ refers to the number of circumferential variations and $m = 1$ refers to the number of radial variations. Within the coax, this mode then becomes the dominant circular waveguide mode to appear [14]. To reduce the propagation of this mode, the ratio of the coaxial transition has to be significantly reduced. In this case, the transition was designed to have an inner diameter of 100 µm and outer diameter of 300 µm; flushed in a 300 µm thick substrate (Figure 1(a)). According to [9], the equation below can be used to determine the characteristic impedance of a coaxial line with a known dielectric constant. Corresponding to a 1 : 3 inner/outer diameter ratio, characteristic impedance ($Z_o$) of 19.2 Ω was calculated using the equation below:

$$Z_o = \frac{60}{\sqrt{\varepsilon_r}} \ln \frac{R_{out}}{R_{in}} \tag{1}$$

where $\varepsilon_r$ is the dielectric constant, $R_{out}$ is the radius of the outer dielectric, and $R_{in}$ is the radius of the inner conductor. The outer conductor of the transition was designed 150 µm thick surrounding the outer coax. To reduce impedance mismatching between the transition and a 50 Ω source, it was suggested that its electrical length be kept as short as possible; therefore the transition was designed flush in the 300 µm substrate. To properly characterize the transition at ports 1 and 2, gold coplanar waveguide (CPW) lines matched at 50 Ω were included on the top and bottom side of the substrate as shown in Figures 1(a) and (b). The dimensions of the CPW lines are $G = 5$ µm

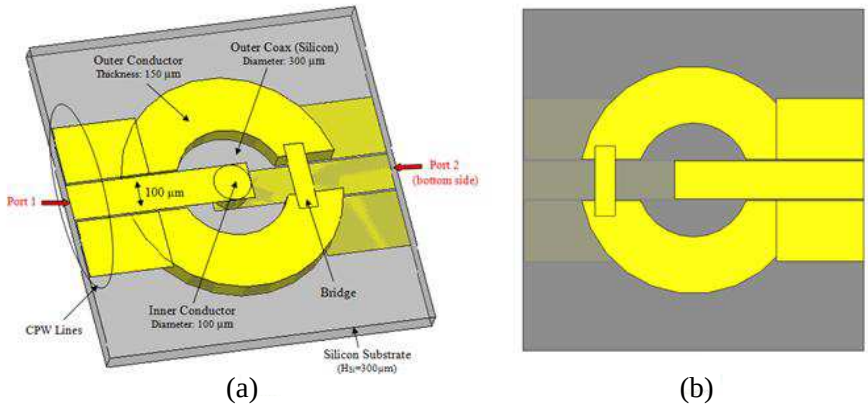



**Figure 1.** A layout of the vertical micro-coaxial transition for high frequency packaging technologies. (a) Top-side view of transition. (b) Backside view of transition.

and $W = 100\,\mu m$, where $G$ is the gap distance between lines and $W$ is the width of the signal line. The width of the CPW ground lines were $160\,\mu m$. The signal lines were connected to the center conductor to transmit the RF signal and the ground lines provided a reference for the outer conductor. To account for the air gap in the outer conductor, gold bridges were used to complete the ground connection.

## 3. FABRICATION METHODS

### 3.1. Through-hole Formation and Metallization Process

The micro-coaxial transition was realized on a 2 inch, $300\,\mu m$ thick, (100) oriented, high resistive silicon wafer. Figure 2 below shows the

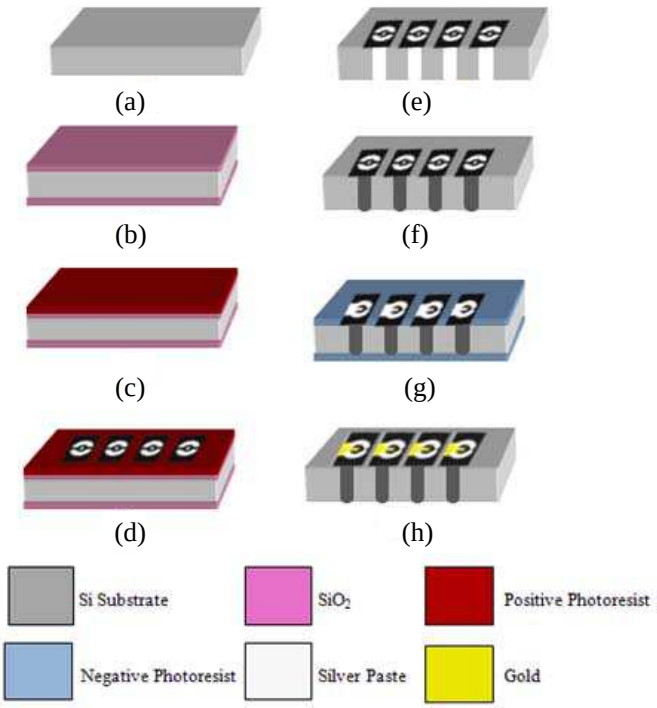



**Figure 2.** Fabrication process sequence for the vertical micro-coaxial transition. (a) Si substrate, (b) $SiO_2$ grown on the substrate, (c) photoresist deposited for patterning, (d) pattern transfer by photolithography, (e) removal of $SiO_2$ layer for etching and coaxial vias formed using deep reactive ion etching, (f) metallization of holes, (g) pattern transfer for CPW lines, and (i) CPW line metal deposition.

steps involved in the fabrication process.

Initially, the silicon substrate was the thermally oxidized on both sides to grow a 1 μm thick $SiO_2$ layer. This oxidation process was required because it served as an etch protective layer to the photoresist during the formation of the through holes. After the oxide growth, the substrate was spin coated with photoresist AZ 4620 (10 μm) on the front side at 500 rpm for 10 seconds; followed by an additional spin step at 1000 rpm for 60 seconds. Following resist coating, the wafer was soft baked for 20 minutes at 100°C. After baking, a 24-hour rehydration process was included in preparation for silicon etching that followed. Using a photomask, the wafer was then exposed with the mask pattern for 13 seconds at 25 mw/cm$^2$ on a Karl Suss mask aligner. The wafer was then placed in a developer solution (AZ 400K 1 : 4) for 4–5 minutes. After developing the pattern, the substrate was hard baked for 30 minutes at 100°C. This step allowed the photoresist to harden and remain on the silicon surface the duration of dry etching.

Next, the coaxial through holes were formed in the silicon substrate using Bosch process for deep reactive ion etching (DRIE) [15]. To accomplish the silicon etching, an Alcatel AMS 100 SDE was used. The DRIE recipe used in this process was: etch step — $SF_6$ at 300 sccm with 3 seconds cycle; passivation step — $C_4F_8$ at 200 sccm and $O_2$ at 20 sccm with 1.4 seconds cycle; pressure — $5.25 \times 10^{-1}$ mTorr; source generator power — 2400 W; substrate holder power — used in pulsed mode, high cycle at 90 W for 20 ms, low cycle at 0 W for 80 ms; substrate holder He pressure — $9.75 \times 10^{-3}$ mTorr. In this process, the wafer was cooled down to −15°C and the 300 μm deep vias where then etched through for 30 minutes; which converted to an etch rate of 10 μm/min. During this etching process, the through holes were formed and the photoresist remained on the silicon surface on the remaining substrate areas. This resist served as a protective layer during the filling of the coaxial transitions.

After the holes were etched through, a metallization step was performed to fill them with a Ferro diluted silver paste [16]. This was achieved using diluted silver paste and a sharp razor blade which coursed the metal into the coaxial holes. In this process, a thick amount of silver paste was applied to the silicon surface and the razor blade was swept across the holes, evenly distributing the metal inside the formed through holes. This step was performed repeatedly to ensure that the metal was being filled not only through the holes, but also along the edges within coaxial structure. Once the filling was complete, the silicon substrate was submerged in acetone to remove the remaining excess silver paste from photoresist surface, leaving only the metalized coaxial transition. Figures 3(a) and (b) illustrate Scanning Electron

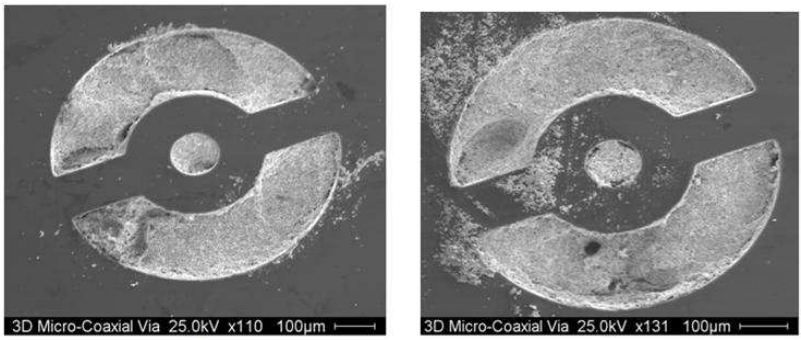



**Figure 3.** SEM images of micro-coaxial transition post through-hole metallization. (a) Front side and (b) backside.

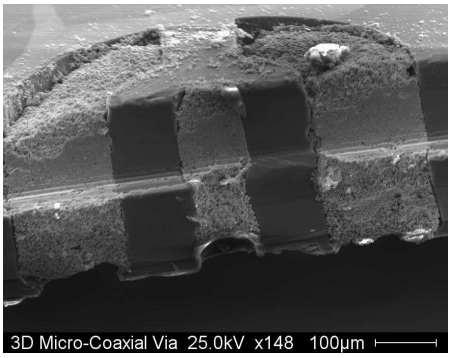



**Figure 4.** Cross-section SEM image of micro-coaxial transition post through-hole metallization.

Microscope (SEM) images of the micro-coaxial transition following a successful metallization process. The image shows front and backside views of the inner and outer coax structure completely filled without the overlapping of silver paste. In order to verify the holes were completely filled through the silicon substrate, a cross-section of the coaxial transitions was taken using the SEM. Figure 4 below illustrates the cross-sectional view of the filled coaxial transition.

### 3.2. Fabrication of CPW Lines

An additional photolithography step was performed to pattern the CPW lines on the top and bottom side of the substrate. The wafer with metalized through holes was spin coated with NR9-3000PY negative photoresist at 1000 rpm for 30 seconds and then soft baked for 1 minute

at 150°C. Next, the wafer was exposed using the Karl Suss mask aligner for 23 seconds at 25 mw/cm$^2$and hard baked for 1 minute at 100°C. The wafer was then developed in RD6 solution for 10 seconds. Following this lithography process, an electron beam evaporator was used to deposit the metal on the CPW line patterns. First a chrome (Cr) layer of ∼15 nm was deposited at a rate of 0.3 A/sec and acted as an adhesion layer for the top gold (Au) layer. The Au layer had a thickness of ∼300 nm and was deposited at a rate of 2 A/sec. Finally, a liftoff process was performed by placing the substrate in acetone overnight which removed the remaining Au from the silicon surface. It is important to note that this entire process was repeated to include the CPW lines on the backside of the wafer. Figures 5(a) and (b) illustrate front and backside microscopic images of the fabricated micro-coaxial transition with gold CPW lines.

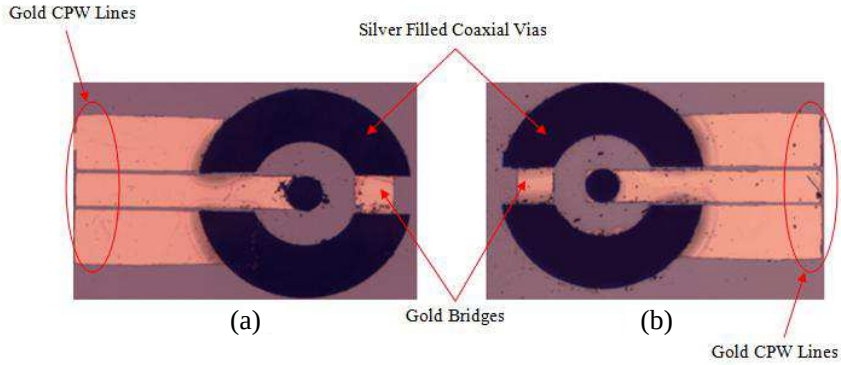



**Figure 5.** Microscopic images of fabricated micro-coaxial transition with gold deposited CPW lines. (a) Front side and (b) backside.

## 4. RF CHARACTERIZATION TECHNIQUES

### 4.1. Measurement Setup

There were several device components that were used to perform the required RF characterization of the coaxial transition. Figure 6 illustrates test setup utilized during the characterization of the micro-coaxial transition.

To determine the reflection coefficient and insertion loss of the coaxial transition, an Anritsu 37397 vector network analyzer (VNA) was used. The measurement setup in the figure above demonstrates the equipment used during RF characterization. The fabricated transition (DUT) was first placed on a Microtech probe station that contained RF

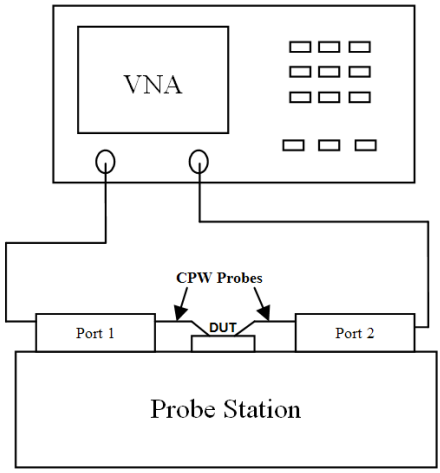



**Figure 6.** Illustration of test setup used for RF characterization of micro-coaxial transition.

ports 1 and 2. Each port was then connected to ground-signal-ground (CPW) Micromanipulator High Frequency Picoprobes [17] using V-band cables, which were capable of measuring up to 67 GHz. Next, a short, open, load, and thru (SOLT) calibration was performed using a CS-5 kit to eliminate any parasitic effects that may affect the measurement results. This calibration removed most of the signal losses present from the VNA ports, to the tip of the ground-signal-ground pitch probes. Finally, the RF characteristics of the transition were measured at high frequencies.

### 4.2. Device Simulation

While attempting to measure the performance of the coaxial transition, it was discovered that port 1 could easily connect to the devices; however, port 2 was impossible to reach due to the CPW lines being located on the backside of the silicon substrate. To accommodate for measurements at port 2, an additional silicon substrate was used to extend the CPW lines on the bottom of the original substrate. To verify the performance of the transition prior to fabricating the additional substrate, the entire design was simulated using Ansys's HFSS [18]. The transition was simulated flushed in a 300 µm thick silicon substrate with an inner and outer diameter of 100 µm and 300 µm. The ground conductor surrounding the outer dielectric was 150 µm thick. The material properties of the silver paste used were uploaded into the simulator and then used as the metal that filled

the inner and outer conductors of the transition. The simulation was performed over a broad frequency range from dc-to-65 GHz, and fed by two wave ports (1 and 2) which were matched to 50 ohms. The additional substrate which included the extended CPW lines was also included in the simulation to investigate losses that would occur when measuring the insertion loss between both ports. This substrate was also designed to be 300 µm thick and included the same CPW line dimensions as those integrated on the front and backside of the transition. The simulated results were then compared to the measured results obtained in Section 5.1.

### 4.3. Additional Substrate Alignment

However, getting the CPW lines on both substrates aligned properly for measuring became another issue. To properly measure the coaxial

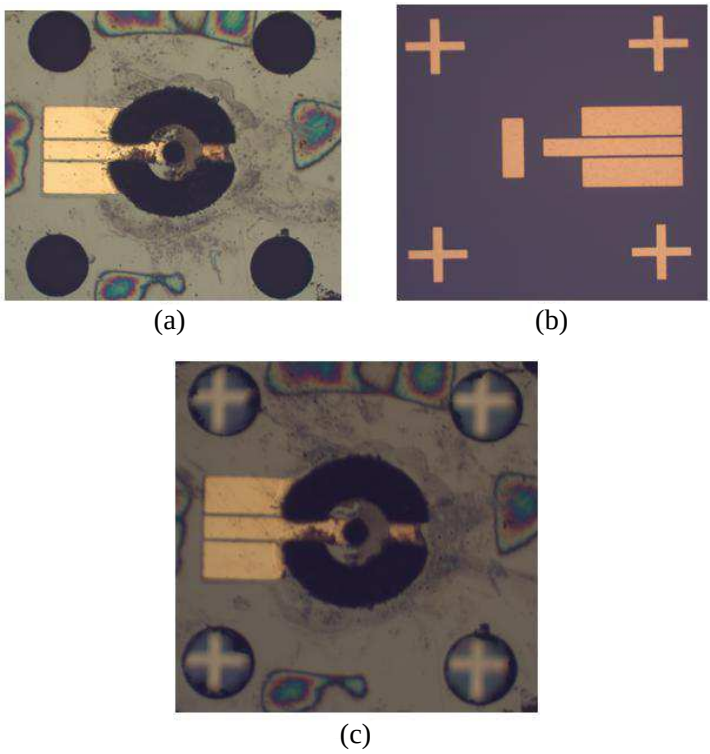



**Figure 7.** Microscopic images of fabricated micro-coaxial transition for integration. (a) Top substrate with etched local alignment holes, (b) additional substrate with cross hairs for extended CPW lines, and (c) substrate Integration using local alignment holes and cross hairs.

transition without any losses present from the CPW line integration, the lines on the backside of the top substrate needed to be carefully aligned to those on the additional substrate. This was achieved by designing two mask layers using AutoCAD [19]: the first mask layer included "local" alignment marks (individual circles) which surrounded the coaxial transition on the top substrate. These local marks were then etched through the substrate and served as windows that allowed a visual to the alignment marks on the additional substrate. Following this, another mask layer was included on the additional substrate which served as "bottom" alignment marks (cross hairs). These mask layers were then integrated by aligning the cross hairs of the "bottom" layer to the circles of the "local" layer. Once these layers were aligned, this verified that the CPW lines were properly aligned to one another and measurements could be made with minimum signal loss present in between lines. These masks layers allowed the coaxial transition to be measured using both ports. Figure 7 illustrates microscopic images of the both substrates used during integration as well as their alignment prior to measuring.

## 5. RF CHARACTERIZATION RESULTS

### 5.1. Measured Reflection Coefficient and Insertion Loss

After properly integrating and aligning the substrates, RF characterization was performed on the coaxial transition. Measurements were performed over a wide frequency range from dc-to-65 GHz. The reflection coefficient and insertion loss of several micro-coaxial transitions were measured to get more accurate results. Measured results were compared to the responses obtained during simulation.

The measured results of four micro-coaxial transitions are shown in Figures 8(a) and (b). It is important to note that all transitions measured were identical and were designed and fabricated with the same inner and outer diameters of 100 µm and 300 µm. When measuring the reflection coefficient, most of the devices seem to demonstrate good results compared to simulations with more than −10 dB loss difference at high frequencies from approximately 15 GHz-to-57 GHz. At lower frequencies (dc-to-10 GHz), however, majority of the signal received from port 1 was reflected back and passed the −10 dB mark, which demonstrates a device short and/or poor signal transmission. Transitions 2 and 3 provided the best results with reflection coefficients greater than −15 dB over 20 GHz bandwidth; only decreasing less than −10 dB at 40, 50, and 60 GHz, increasing the operating frequency range achieved in previous work [20]. Transitions 1

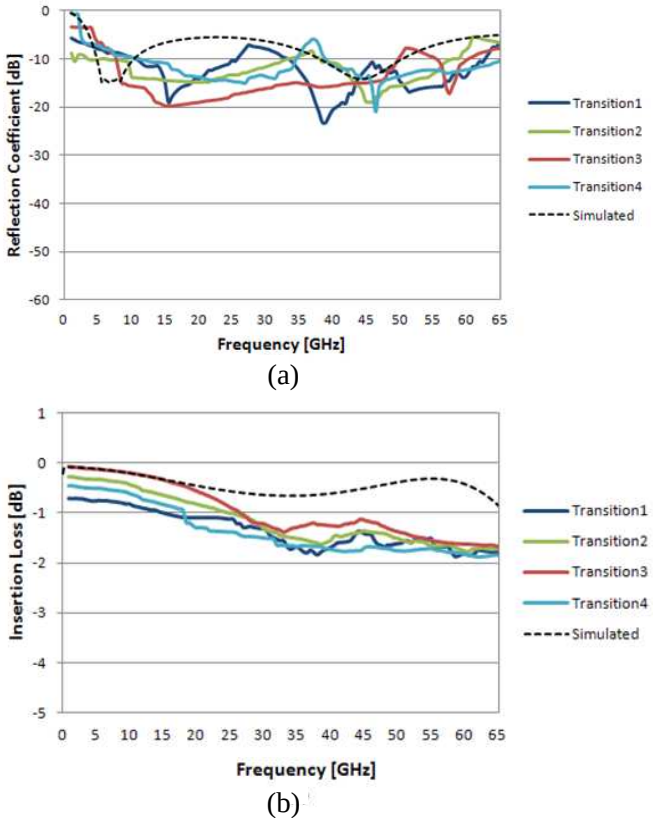



**Figure 8.** Measured results of micro-coaxial transition vs. simulated response with substrate integration. (a) Reflection coefficient and (b) insertion loss.

and 4 had good reflection as well but did not sustain performance over a wide frequency range.

However, some design issues that were discovered during fabrication affected the reflection coefficient of the transition device. For example, the CPW lines on the front and backside on the coaxial transitions were designed with a 5 µm gap between signal and ground. This caused major issues when the transitions were fabricated because the through holes that were etched in the silicon substrate created a non-uniform surface which prevented the photoresist from being evenly distributed for the CPW line pattern. Therefore, when the CPW line pattern was developed, some areas in between the signal and ground lines were poorly covered with photoresist. This caused an immediate device shortage for some transitions because following the

gold deposition of the lines, areas not covered with resists contained particles of gold after liftoff. Although the resist spin recipe was adjusted to achieve the desired results, a slight design adjustment to increase the CPW line gap distance would reduce fabrication issues. Also, having to include an additional substrate during integration caused additional heating on the substrate after the CPW lines were patterned to include the local holes. This caused a slight shrinkage in the gold lines on the surface which reduced the performance of the transition. These adjustments would improve the reflection coefficient results obtained for the micro-coaxial transition.

The measured results for the insertion loss of the coaxial transitions are shown in Figure 8(b) above. It can be seen that all four devices behaved well from dc-to-35 GHz, demonstrating less than $-1.5$ dB, which was very close to the simulated results. This proves that the transitions have good signal transmission between the two ports and would provided minimal loss when integrated with other multi-layer high frequency devices. Beyond 35 GHz however, the transitions performance began to decrease, nearly reaching $-2$ dB of insertion loss. This behavior did not agree well with simulation, where the insertion loss was nearly $-0.5$ dB from 50-to-65 GHz. This was a critical discovery because it altered the transitions signal transmission abilities at higher frequencies. Since the transition was specifically designed to behave well over a wide range of high frequencies, further studies were conducted to determine the cause of the degrading signal.

During the substrate alignment for measuring, it was discovered that even when the local holes were centered with the bottom cross hairs, a slight misalignment still occurred. This is due to the fact that while the transitions were being measured, the top substrate shifted slightly because of the pressure of applied from the CPW probes. This minor shift caused the CPW lines on the backside of the top substrate to misalign with the extended CPW lines on the additional substrate by about 2–3 μm, which is perceived to be what created the discrepancy between the measured and simulated data. This misalignment and shift of the top and bottom substrates can be seen in Figure 9. The figure shows that the bottom hairs were not consistently centered with the local holes during measuring, which caused additional capacitances to appear between the CPW signal and ground lines on the additional substrate. These capacitances ultimately disrupted the behavior of the signal being evaluated from port 2.

To verify this assumption, an additional simulation was performed in HFSS for the insertion loss response when the two substrates were slightly misaligned. The measured insertion loss data was then compared to the substrate integrated and misaligned simulated results.

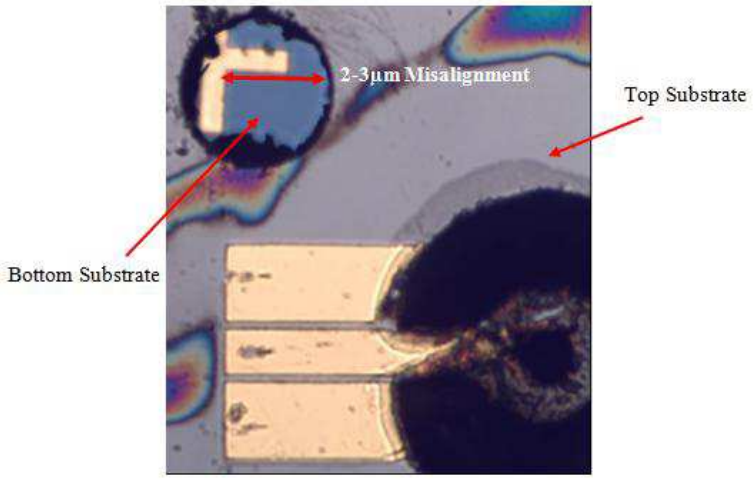



**Figure 9.** Microscopic image of top and bottom substrate misalignment during measuring.

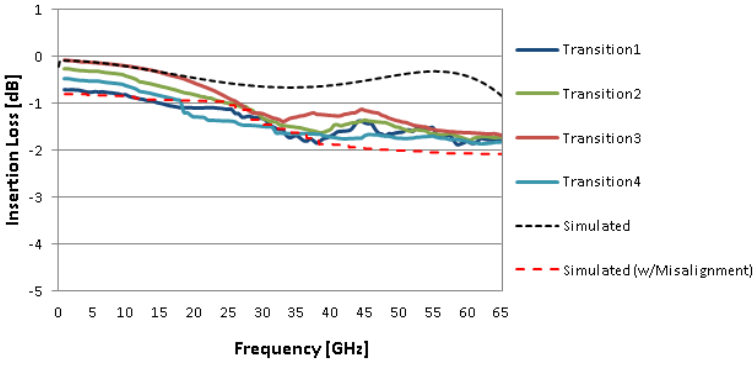



**Figure 10.** Measured insertion loss of micro-coaxial transition compared to additional substrate integration and misalignment.

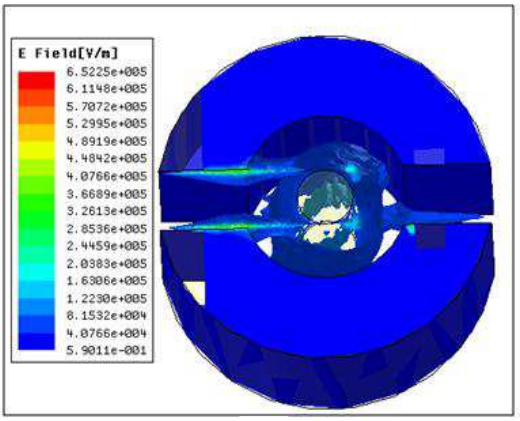
Figure 10 illustrates the insertion loss results when the top and bottom substrates were misaligned by 2–3 µm.

It can be seen above that the measured data did agree with the misaligned simulated results by decreasing at higher frequencies. The measured results now closely resemble the behavior obtained during the misalignment simulation at high frequencies; therefore, it was determined that the variance between the integrated simulation and measured data was due to a misalignment with both substrates.

### 5.2. Field Distribution Analysis

Additionally, the electromagnetic behavior within the coaxial transition was investigated as well as the current distribution along the CPW lines using the HFSS software. The electromagnetic distribution within the transition is shown in Figures 11(a) and (b) below.

(a)




(b)

**Figure 11.** Simulated electromagnetic distribution of the micro-coaxial transition. (a) Along CPW signal lines and (b) within coaxial structure.

The illustrations above demonstrate the current traveling within the electric field of the coax and CPW lines. The ports provided the excitation of current, allowing it to travel through the coax from one signal line to the next. The lighter colored regions indicate maximum current flow through the transmission lines. These lines behaved as inductors and the gaps in between the CPW lines produced a capacitance. The focus of the electromagnetic field however, was within the coaxial region as shown in Figure 11(b) where the current distribution surrounded the inner conductor. This occurred because the inner conductor behaved as an inductor; which had resistance due to the resistivity of the silver used during simulation. The outer conductor in this case was silicon since the transition was designed flush in the substrate. Therefore, the interaction between the inner

conductor and outer dielectric also produced a capacitance in the coaxial structure.

## 6. CONCLUSION

In summary, several through wafer vertical micro-coaxial transitions were designed flushed in a silicon substrate with identical dimensions. The coaxial structure was designed to operate at high frequencies and simulated using HFSS. The fabrication techniques were identified and the transitions were developed using standard photolithography. The transition vias were filled with silver paste using a novel approach and the CPW lines were fabricated using e-beam deposition. Finally, four transitions were measured to determine their reflection coefficient and insertion loss response. Results confirmed that the transitions had good behavior when transmitting a RF signal between two ports demonstrating reflection coefficients greater than $-15$ dB over 45 GHz bandwidth; only decreasing less than $-10$ dB at 40, 50, and 60 GHz. The results also showed that the insertion loss of the transitions behaved well from dc-to-40 GHz, demonstrating less than $-1.5$ dB. These results verified that the micro-coaxial transition can successfully be integrated in millimeter wave packaging technologies as high frequency transitions. By eliminating the need for thermal or compression bonding, the transition presents a low-cost and durable design that can produce high input/output ratios that are ideal for commercial products.

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